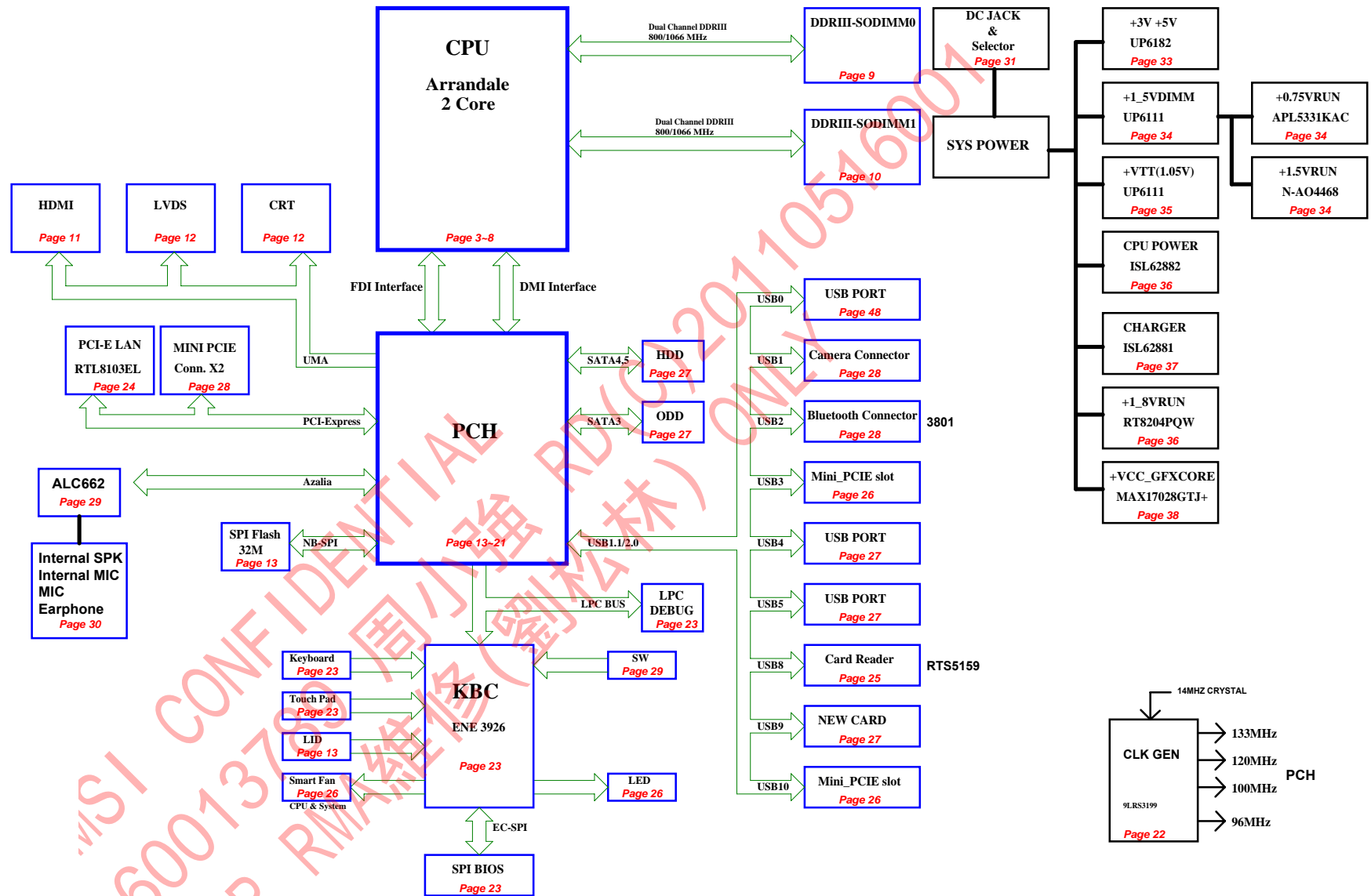


## Calpella Platform

## Table of Contents

## Page Description

01_Block Diagram
02_Platform
03_PROCESSOR-1 (HOST BUS)
04_PROCESSOR-2 (DDR3)
05_PROCESSOR-3 (POWER)
06_PROCESSOR-4 (GRAPHICS POWER)
07_PROCESSOR-5 (GND)
08_PROCESSOR-6 (RESERVE)
09_DDR3 SODIMM 0
10_DDR3 SODIMM 1
11_HDMI & SWITCH
12_CRT,LVDS connector & LID
13_PCH-1 (HDA,JTAG,SATA)
14_PCH-2 (PCI-E,SMBUS,CLK)
15_PCH-3 (DMI,FDI,GPIO)
16_PCH-4 (LVDS,DDI)
17_PCH-5 (PCI,USB,NVRAM)
18_PCH-6 (GPIO,VSS_NCTF,RSVD)
19_PCH-7 (POWER)
20_PCH-8 (POWER)
21_PCH-9 (GND)
22_Clock Generator(9LRS3199AKL)
23_KBC/EC/uP (KB3926)
24_PCI-E 10/100 Lan (RTL8103EL)
25_Cardreader (RTS5159)
26_FAN,LED,Launch board conn
27_HDD,CDROM,USB ,NEW CARD
28_MINI_PCIE,CAMERA,BLUETOOTH
29_AUDIO(ALC662) / AMP(APA2031)
30_SPK & HP & MIC
31_M_Battery select
32_M_Battery Charger
33_M_System Power
34_M_SMDDR_VTERM /1.5VRUN
35_M_VTT Power,+1.8VRUN
36_M_CPU power
37_M_Graphic Core
38_Screw / EMI
39_1681A_USB BOARD
40_1681B_Touch Pad Board
41_Power on Sequency
42_Power down Sequency
43_Power MAP



SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

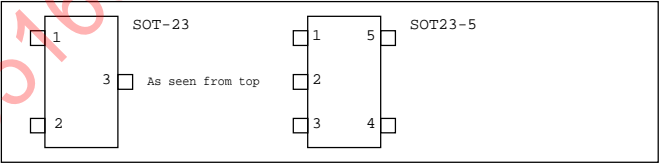
Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
PWR_SRC	19V	S0,(S3-S5)	LAN
+5VALW	5V	S0,(S3-S5)	
+5VRUN	5V	S0	
+5VSUS	5V	S0	
+3VALW	3.3V	S0,(S3-S5)	
+3VSUS	3.3V	S0,(S3-S5)	DDRIII core
+3VRUN	3.3V	S0	
+1_5VDIMM	1.5V	S0,S3	
+1_5VRUN	1.5V	S0	PCH DDRIII command & control pull up. CPU core rail Graphics core rail ( Dual Core only )
VTT	1.05V	S0	
+0_75VRUN	0.75V	S0	
+VCC_CORE	1.05V~1.1V	S0	
+VCC_GFXCORE	1.1V	S0	

Net Naming Conventions

<b>Suffix</b>
# = Active Low Signal
<b>Prefix</b>
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints



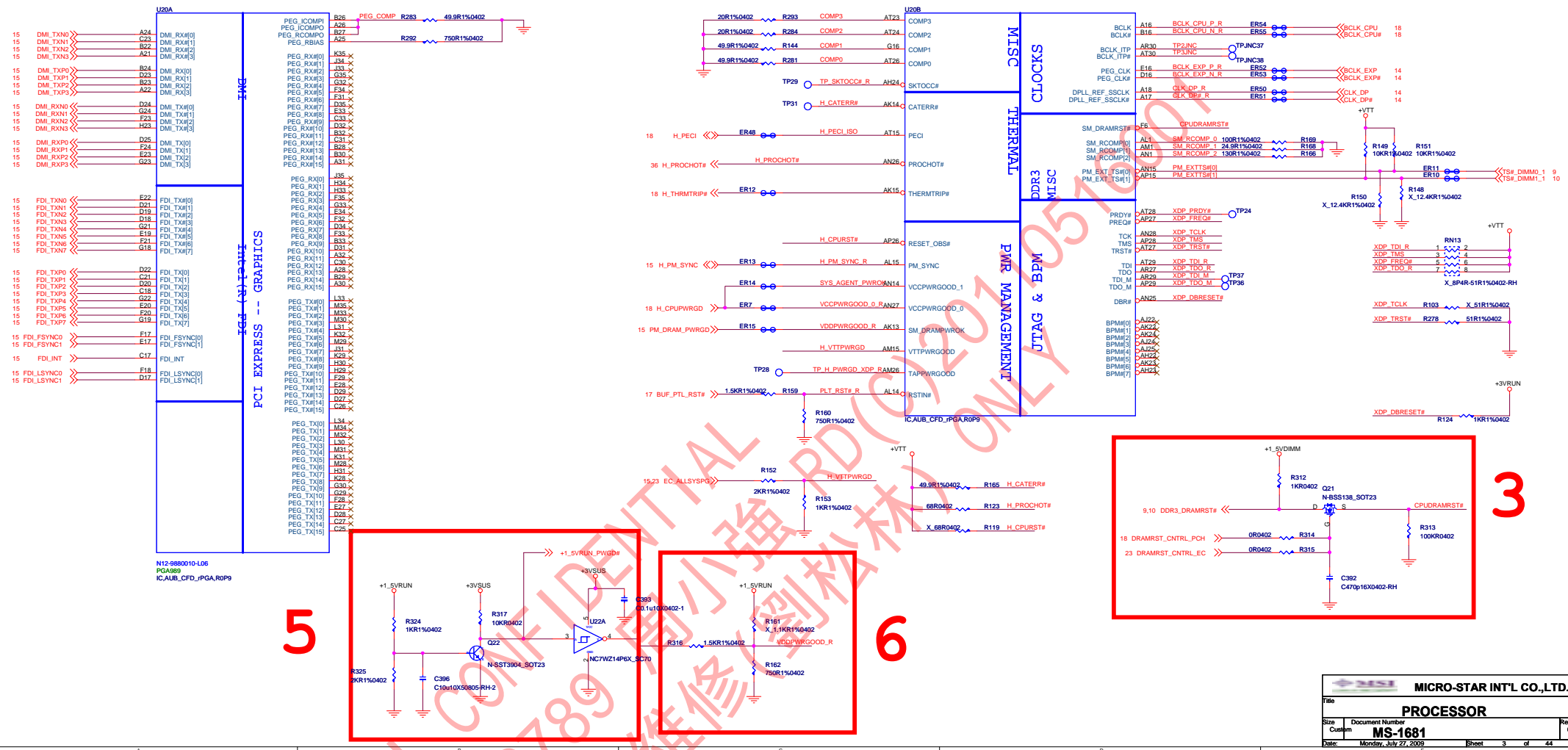
AC Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF

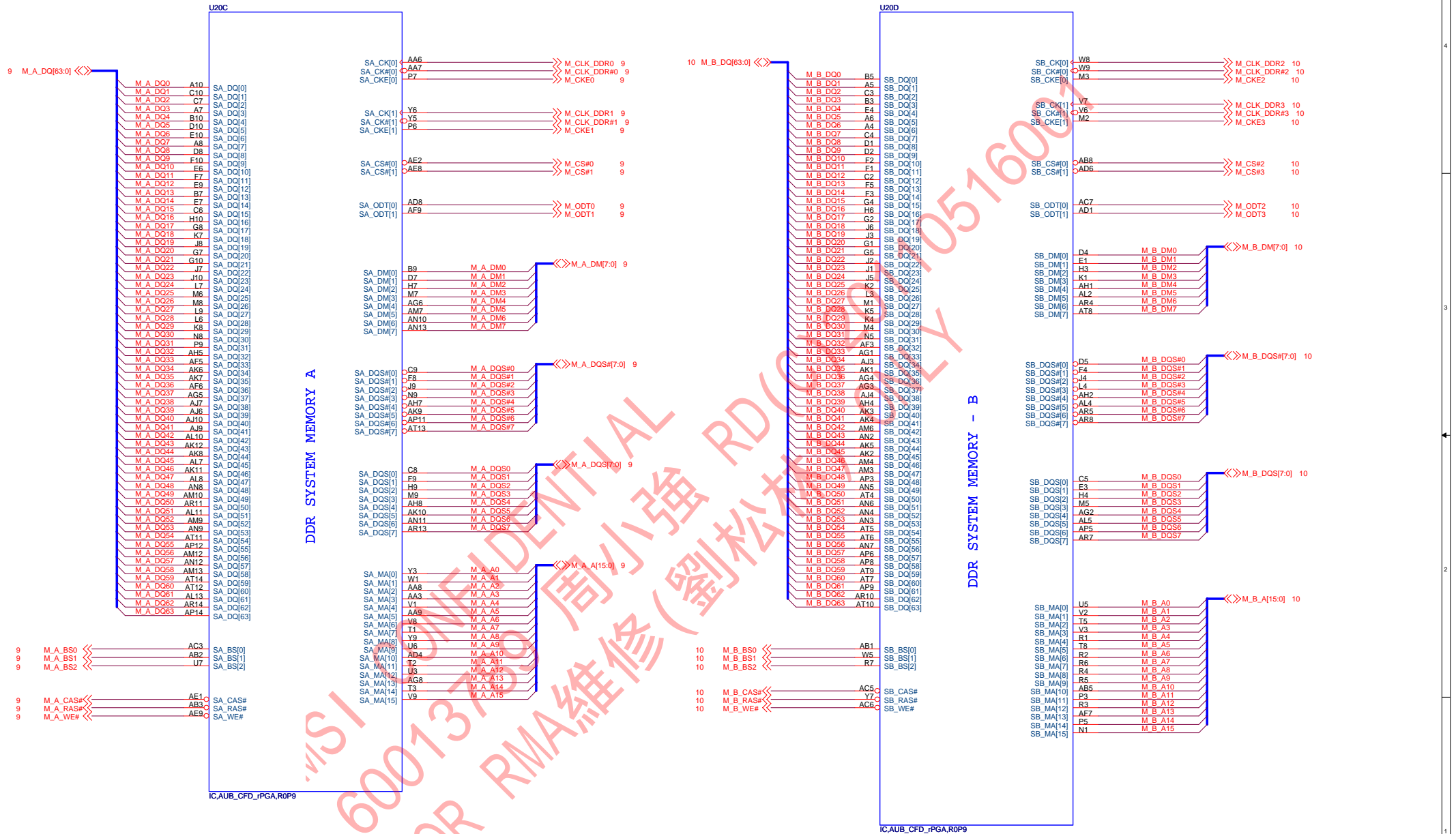
Battery Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF

## ARRANDALE PROCESSOR (CLK,MISC,JTAG)



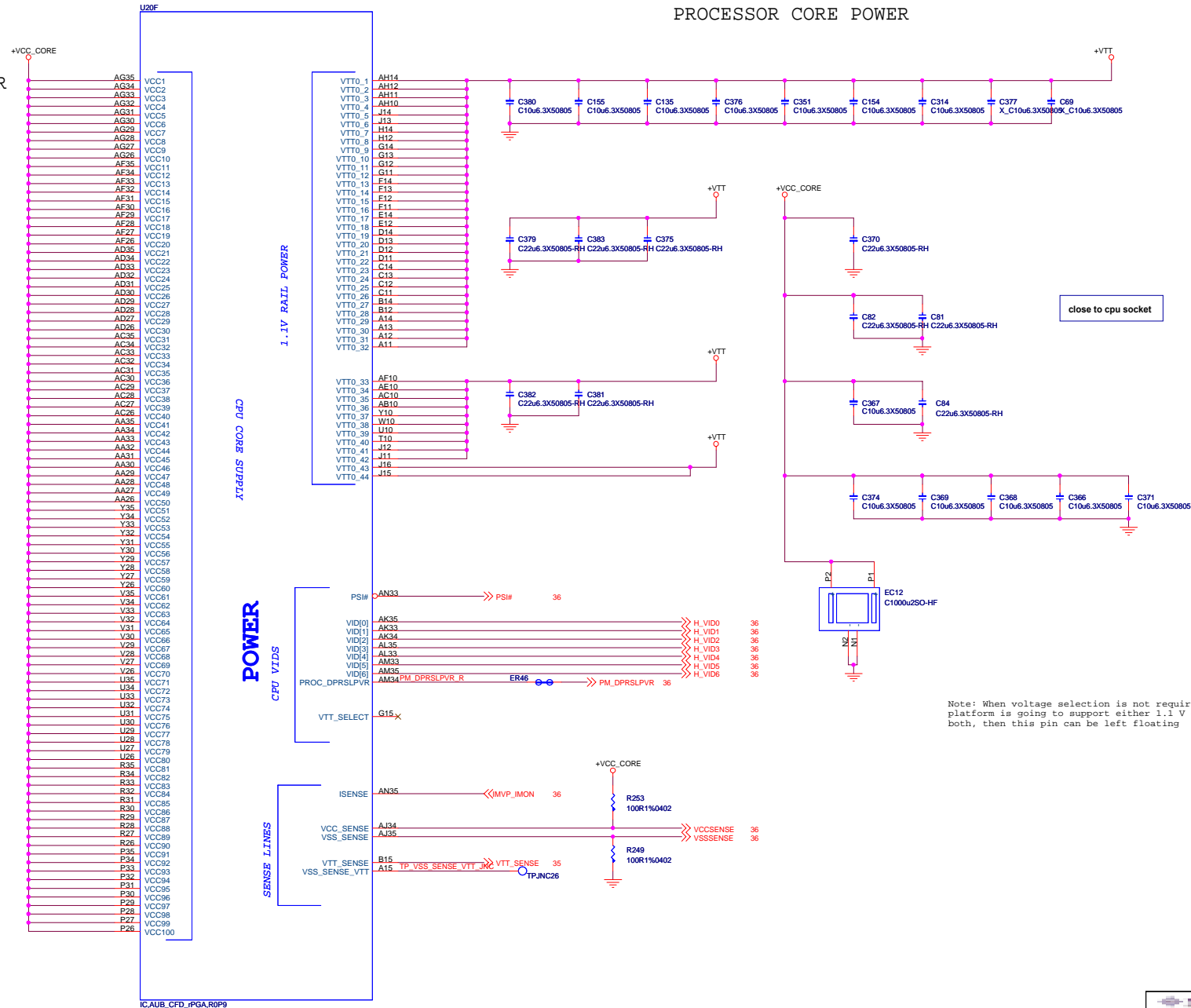
# ARRANDALE PROCESSOR (DDR3)



# ARRANDALE PROCESSOR (POWER)

## PROCESSOR CORE POWER

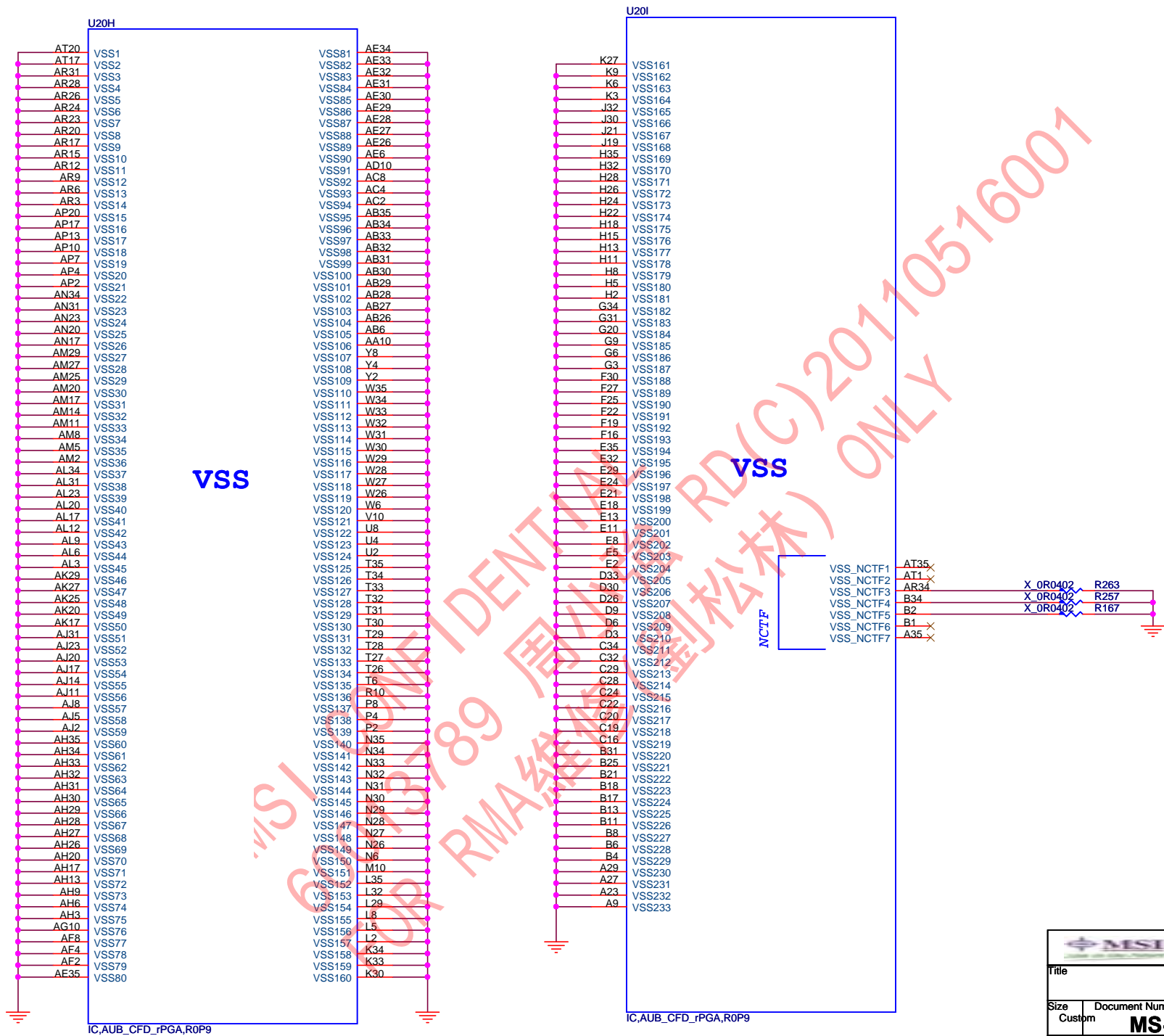
## PROCESSOR CORE POWER



Note: When voltage selection is not required and the platform is going to support either 1.1 V or 1.05 V and not both, then this pin can be left floating



# ARRANDALE PROCESSOR (GND)



RESERVED

RSVD38  
RSVD39

RSVD\_NCTF\_40  
RSVD\_NCTF\_41  
RSVD\_NCTF\_42  
RSVD\_NCTF\_43

RSVD45  
RSVD46  
RSVD47  
RSVD48  
RSVD49  
RSVD50  
RSVD51  
RSVD52  
RSVD53  
RSVD\_NCTF\_54  
RSVD\_NCTF\_55  
RSVD\_NCTF\_56  
RSVD\_NCTF\_57  
RSVD58

RSVD\_TP\_59  
RSVD\_TP\_60  
KEY  
RSVD62  
RSVD63  
RSVD64  
RSVD65

RSVD\_TP\_66  
RSVD\_TP\_67  
RSVD\_TP\_68  
RSVD\_TP\_69  
RSVD\_TP\_70  
RSVD\_TP\_71  
RSVD\_TP\_72  
RSVD\_TP\_73  
RSVD\_TP\_74  
RSVD\_TP\_75

RSVD\_TP\_76  
RSVD\_TP\_77  
RSVD\_TP\_78  
RSVD\_TP\_79  
RSVD\_TP\_80  
RSVD\_TP\_81  
RSVD\_TP\_82  
RSVD\_TP\_83  
RSVD\_TP\_84  
RSVD\_TP\_85

VSS

AP34

0R0402 R259

Vss (AP34) can be left NC  
is CRB implementation;  
EDS/DG recommendation to GND

API  
AT2  
AT3  
ARI

H\_RSVD40

TP42

PCI-Express Configuration Select

CFG0

1:Single PEG  
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

CFG3

1:Normal operation  
0:Lane Numbers Reversed  
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

CFG4

1:Disabled: No Physical Display Port  
attached to Embedded Display Port  
0:Enabled: An external Display Port  
device is connected to the Embedded  
Display Port

Layout Note:  
Location of all CFG strap resistors needs  
to be close to trace to minimize stub

CFG0

NO\_STUFF

R97  
X\_3.01KR1%0402

CFG3

NO\_STUFF

R98  
X\_3.01KR1%0402

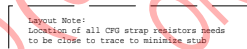
CFG4

NO\_STUFF

R99  
X\_3.01KR1%0402

CFG[3] - PCI Express\* Stat  
Numbering Reversal. Lane R  
applied across all 16 Lane  
1: No lane reversal  
0: Reversal

CONFIDENTIAL 周小強 RD(C)20170516007  
FOR RMA維修(劉松林)

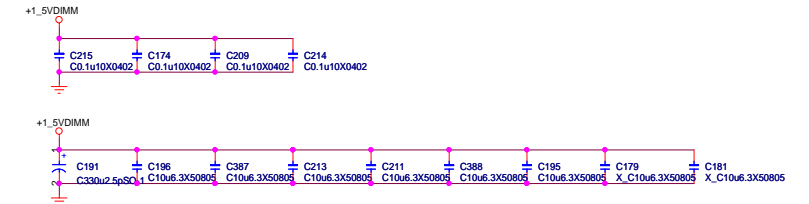
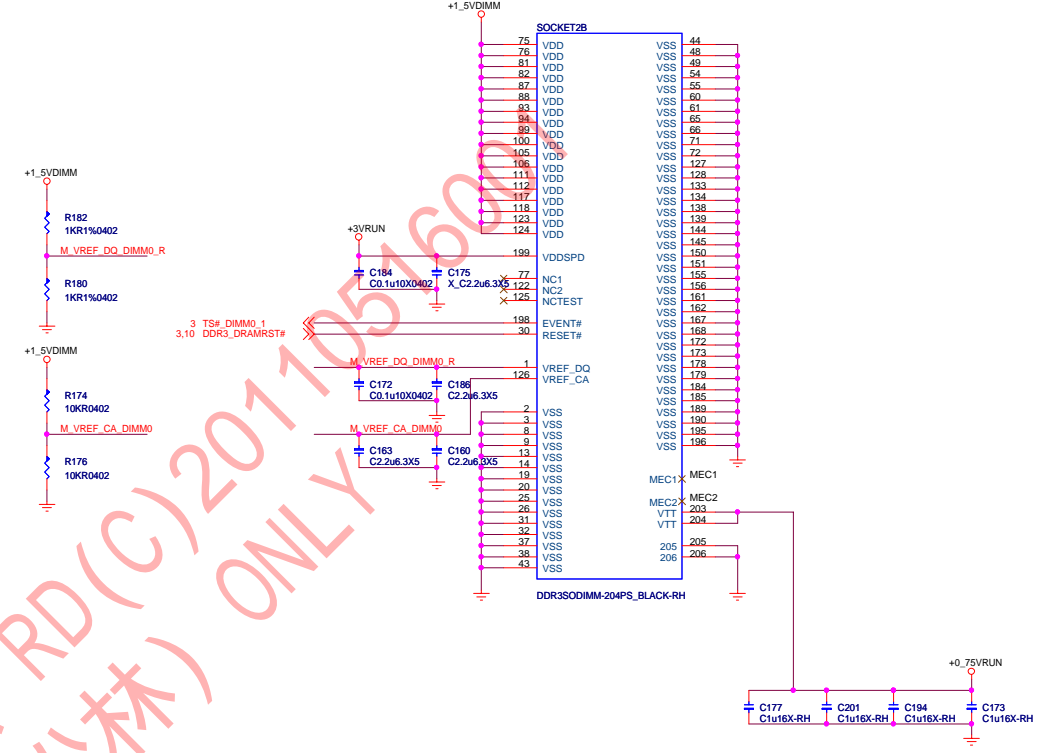
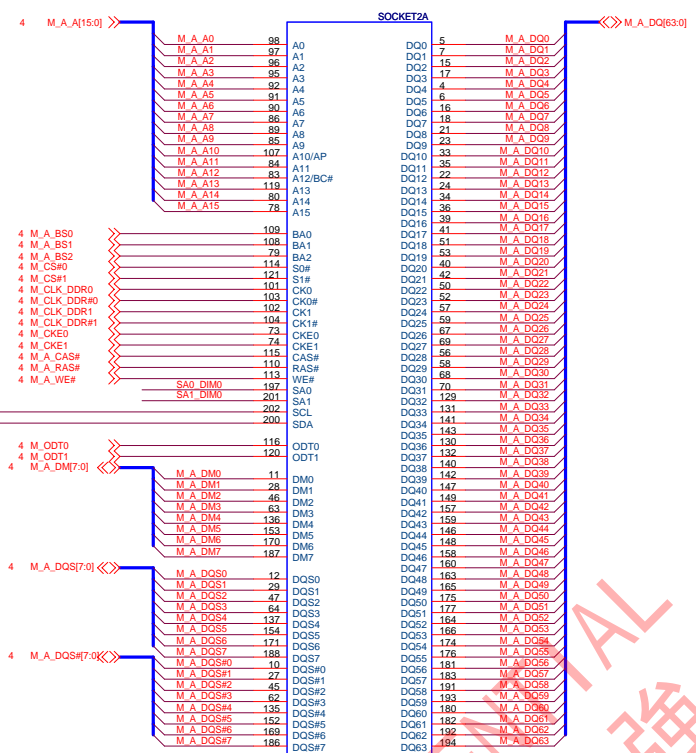


Layout Note:  
Location of all CFG strap resistors needs  
to be close to trace to minimize stub

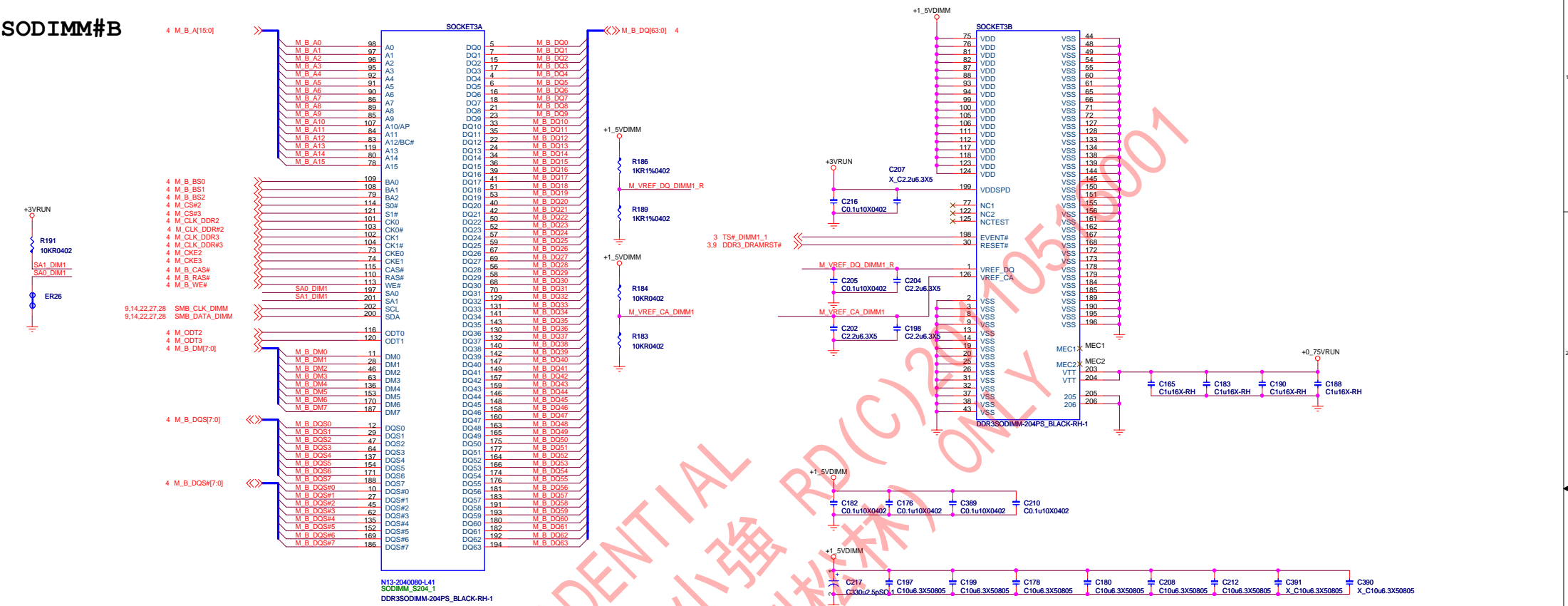
Vss (AP34) can be left NC  
is CRB implementation;  
EDS/DG recommendation to GN



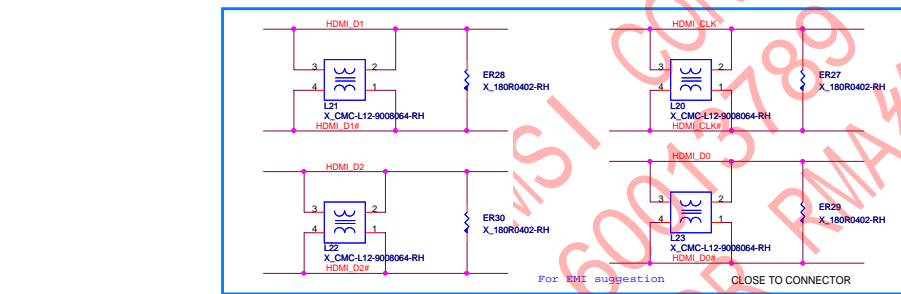
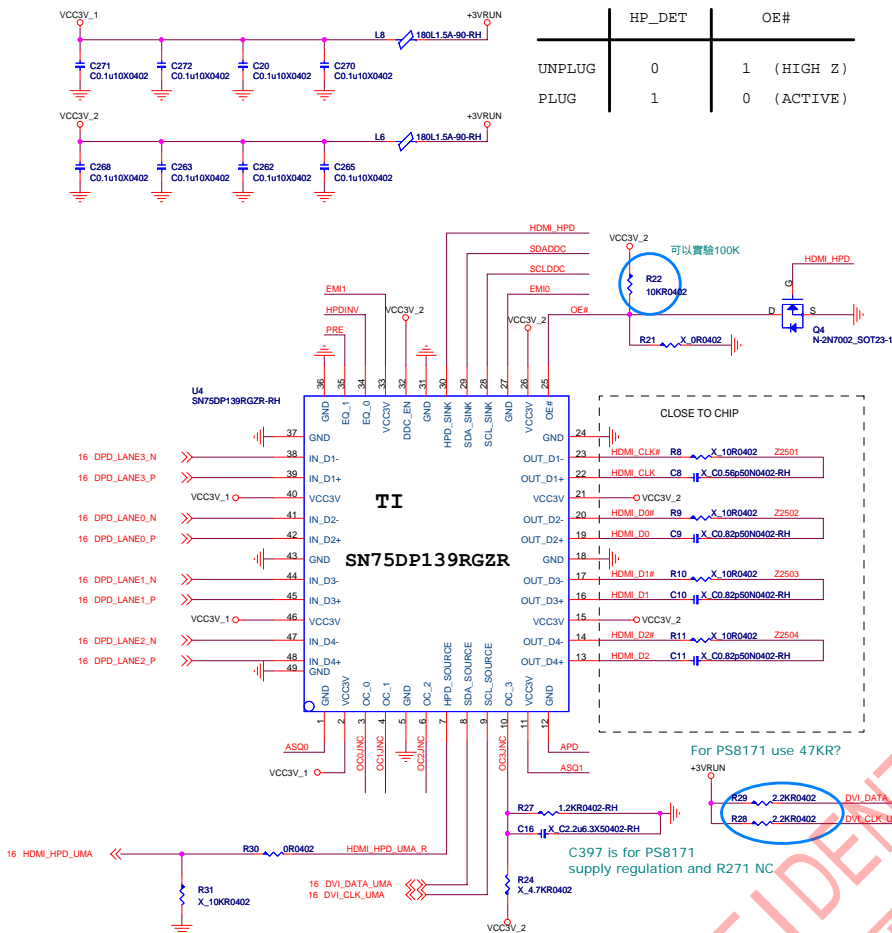
**SODIMM#A**



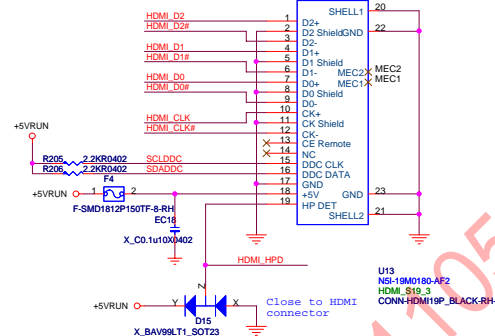
SODIMM#B



# HDMI Switch

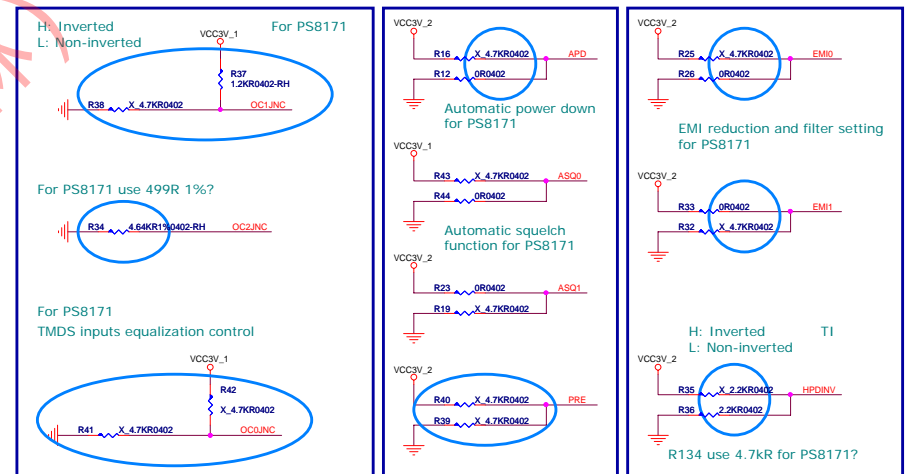


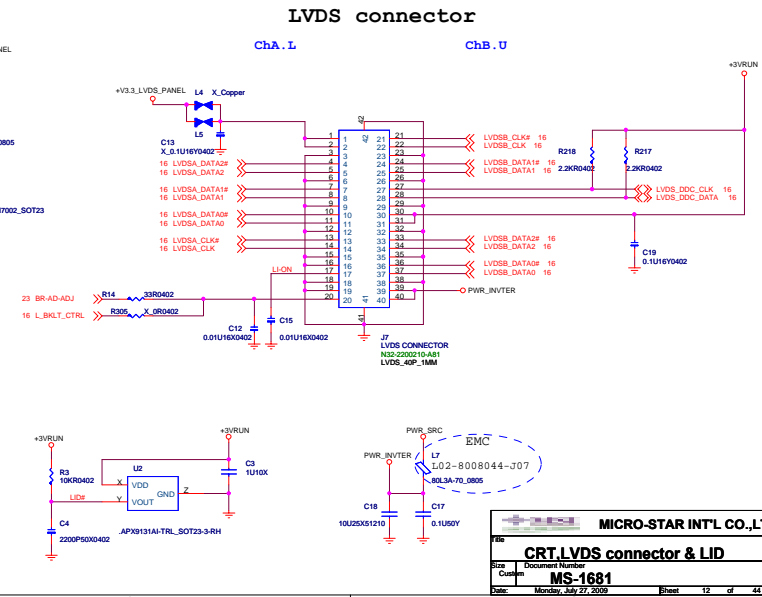
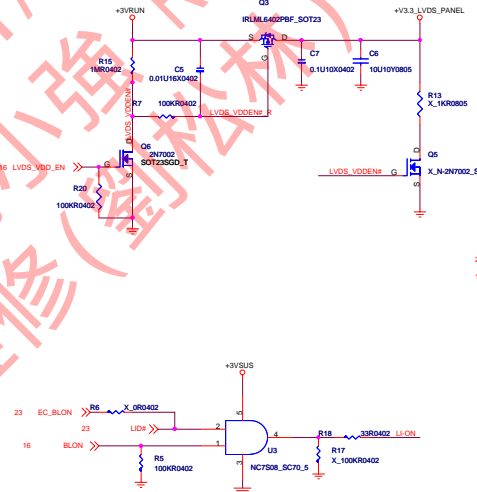
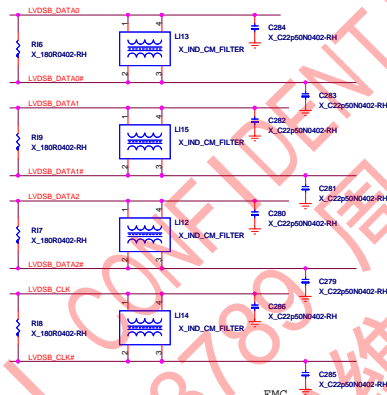
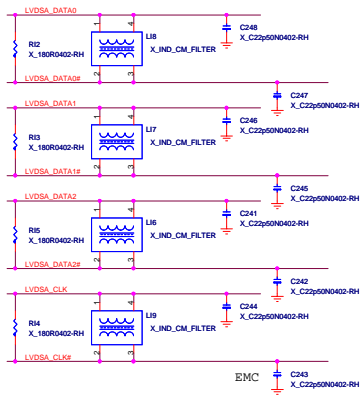
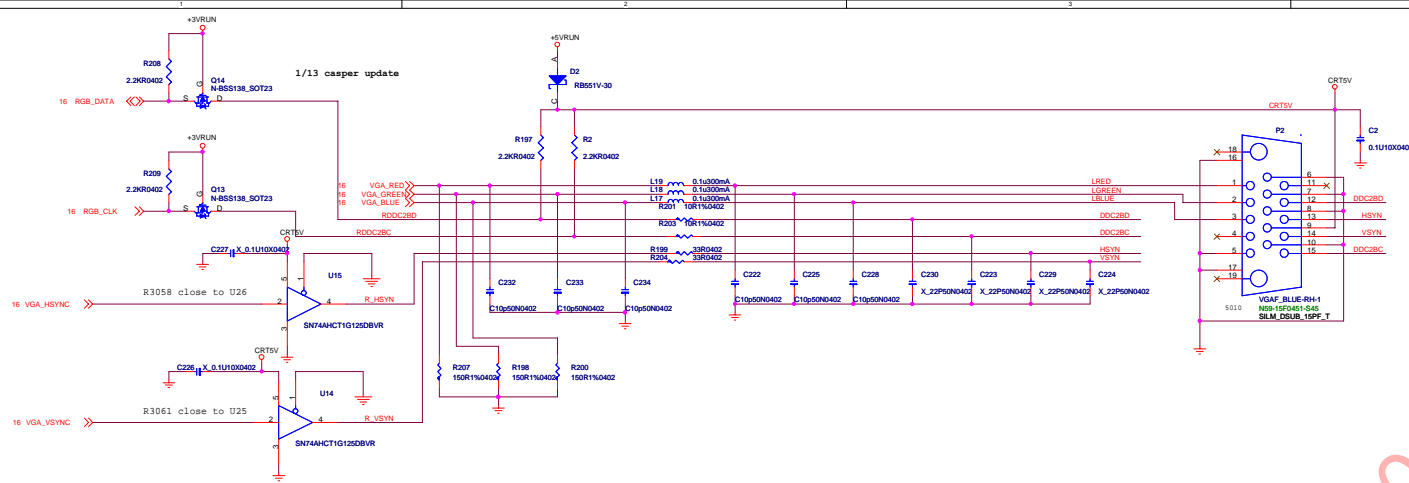
## HDMI connector

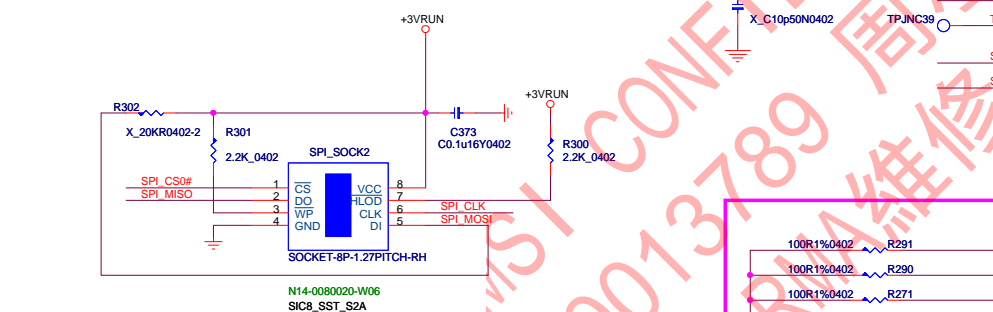
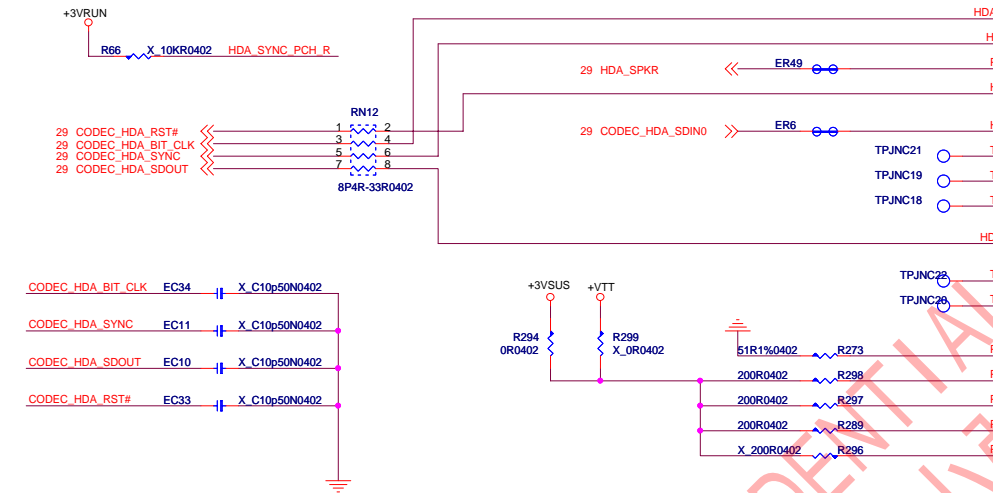


SN75DP139	PS8171	Pin no.
Floating	TMDS inputs equalization control (internal pull-down=500KΩ) PEQ = LOW: Mid level EQ (Default) PEQ = HIGH: High level EQ PEQ = MID: Low level EQ	Pin 3
High	(Internal pull down=500KΩ) PIO = LOW: HPD = HPD_SINK @ 3.3V CMOS output PIO = High: HPD = HPD_SINK# (inverted HPD) @ 0.9V	Pin 4
GND	[ASQ1.ASQ0] = HL: No automatic squelch (Internal pull down=500KΩ) LL: Automatic squelch enable, Level = 120mVpp, default timer LH: Automatic squelch enable, Level = 100mVpp, default timer HH: Automatic squelch enable, Level = 80mVpp, default timer ML: Automatic squelch enable, Level = 120mVpp, extended timer MH: Automatic squelch enable, Level = 100mVpp, extended timer LM: Automatic squelch enable, Level = 80mVpp, extended timer HM: Reserved MM: Reserved	Pin 1 Pin 11
4.65K to GND	499R to GND	Pin 6
GND	Automatic power down management (Internal pull up=500KΩ) APD = LOW: Automatic power down disable APD = HIGH: Automatic power down enable APD = MID: Reserved	Pin 12
1.2K to GND	2.2uF to GND	Pin 10
GND	EMI reduction and filter setting: (EMI1 internal pull up=500KΩ; EMI0 internal pull down=500KΩ) [EMI1,EMI0] = HL: No EMI reduction EMI0 = HIGH: Reduced rise/fall time MID: Reduced rise/fall time, 2nd EMI1 = LOW: EMI filter setting 1 MID: Reserved	Pin 27 Pin 33
Note2	DDC Active Buffer enable and setting (Internal pull-down=500KΩ) DDCBUF = LOW: No DDC active buffer, passive DDC level shifting DDCBUF = HIGH: Active DDC buffer enable, setting 1 DDCBUF = MID: Active DDC buffer enable, setting 2	Pin 34
Floating	TMDS output driver pre-emphasis level setting (internal pull down=500KΩ) PRE = LOW No pre-emphasis PRE = HIGH: Low level pre-emphasis is added PRE = MID: High level pre-emphasis is added	Pin 35

Note2: High is HPD logic inverted, Low is HPD logic non-inverted





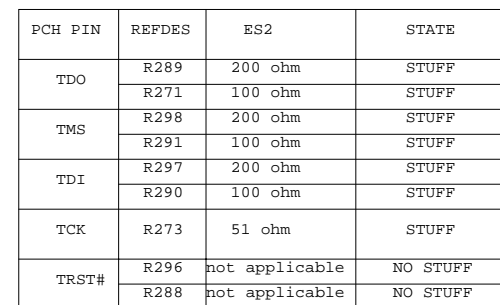
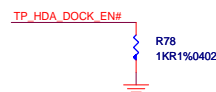
[illegible]

Timing diagram for PCH signals:

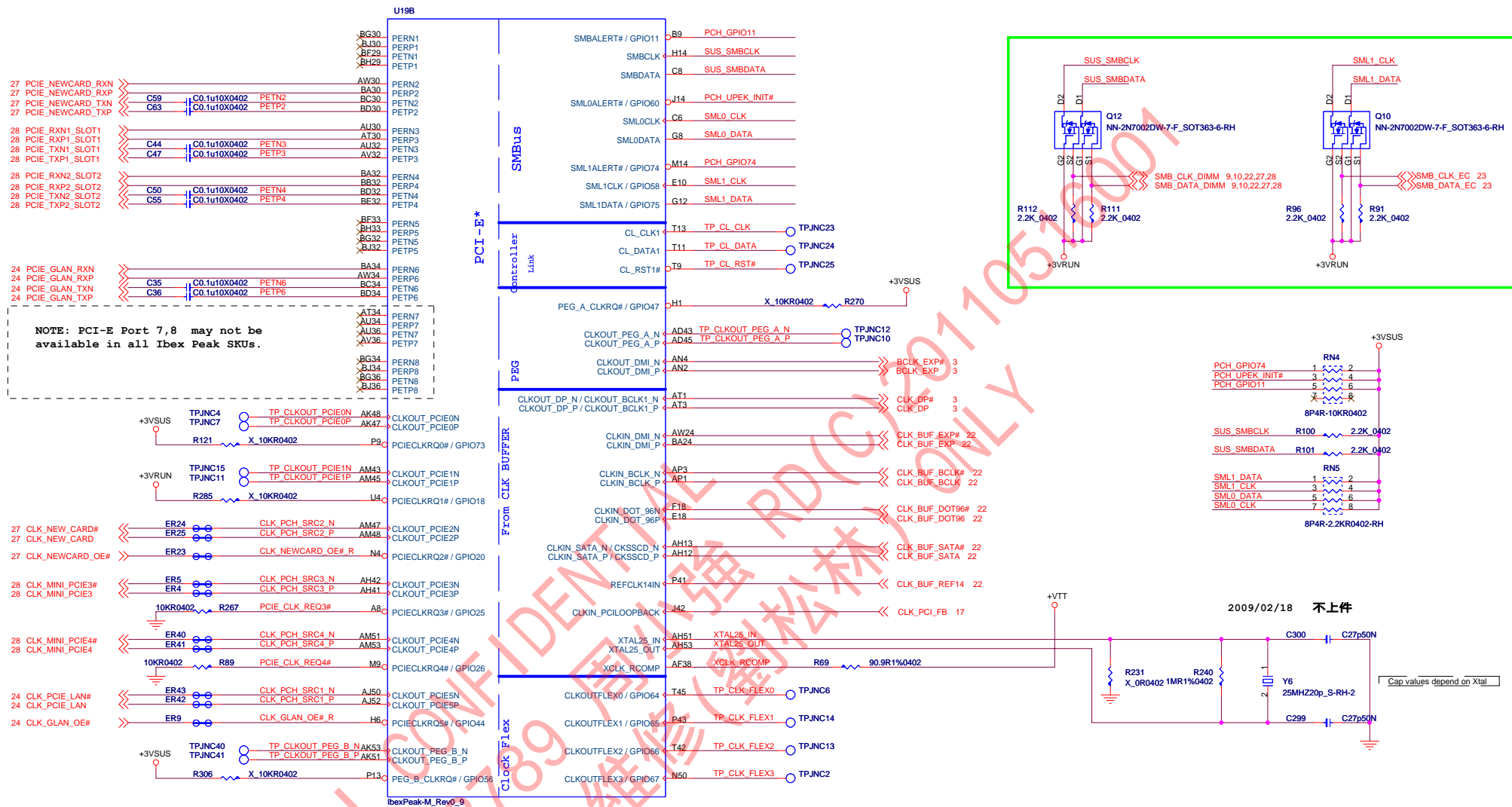
- 100R1%0402 R291 PCH\_JTAG\_TMS
- 100R1%0402 R290 PCH\_JTAG\_TDI
- 100R1%0402 R271 PCH\_JTAG\_TDO
- X 100R1%0402 R288 PCH\_JTAG\_RST#

2009/03/17 修改 for PCH( ES2)

2009/02/08 修改 for PCH( ES2)



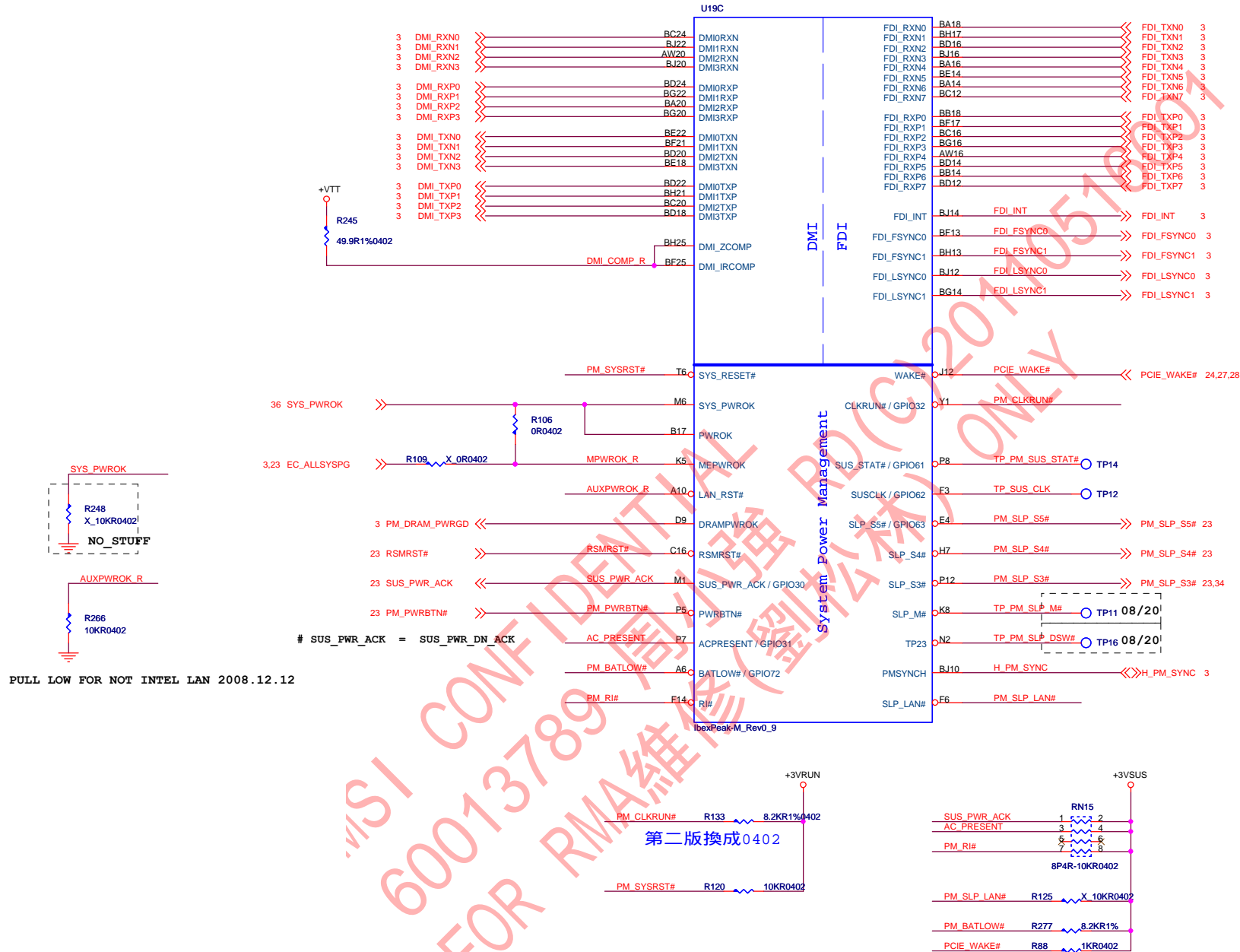
# IBEXPEAK - M (PCI-E, SMBUS, CLK)



PCIECLKRQ1# / GPIO18 PCIECLKRQ1# / GPIO20	RUN Well
PCIECLKRQ0# and PCIECLKRQ3# ~ PCIECLKRQ7# PEG_A_CLKRQ# PEG_B_CLKRQ#	SUS Well

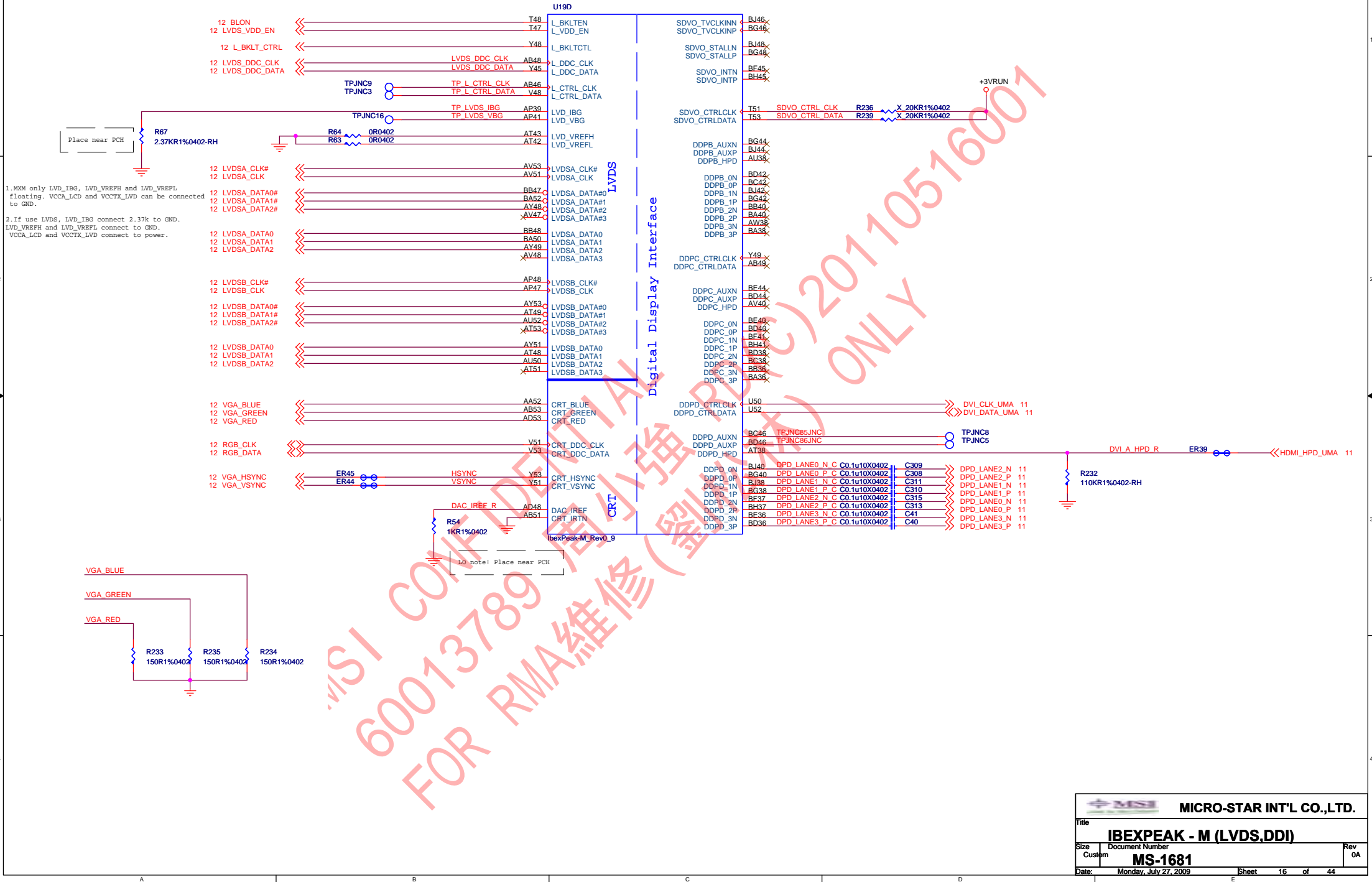
MICRO-STAR INT'L CO.,LTD.			
IBEXPEAK - M (PCI-E,SMBUS,CLK)			
Size	Document Number	Rev	
Custom	MS-1681	0A	
Date:	Monday, July 27, 2009	Sheet	14 of 44

# IBEXPEAK - M (DMI, FDI, GPIO)





# IBEXPEAK - M (LVDS,DDI)

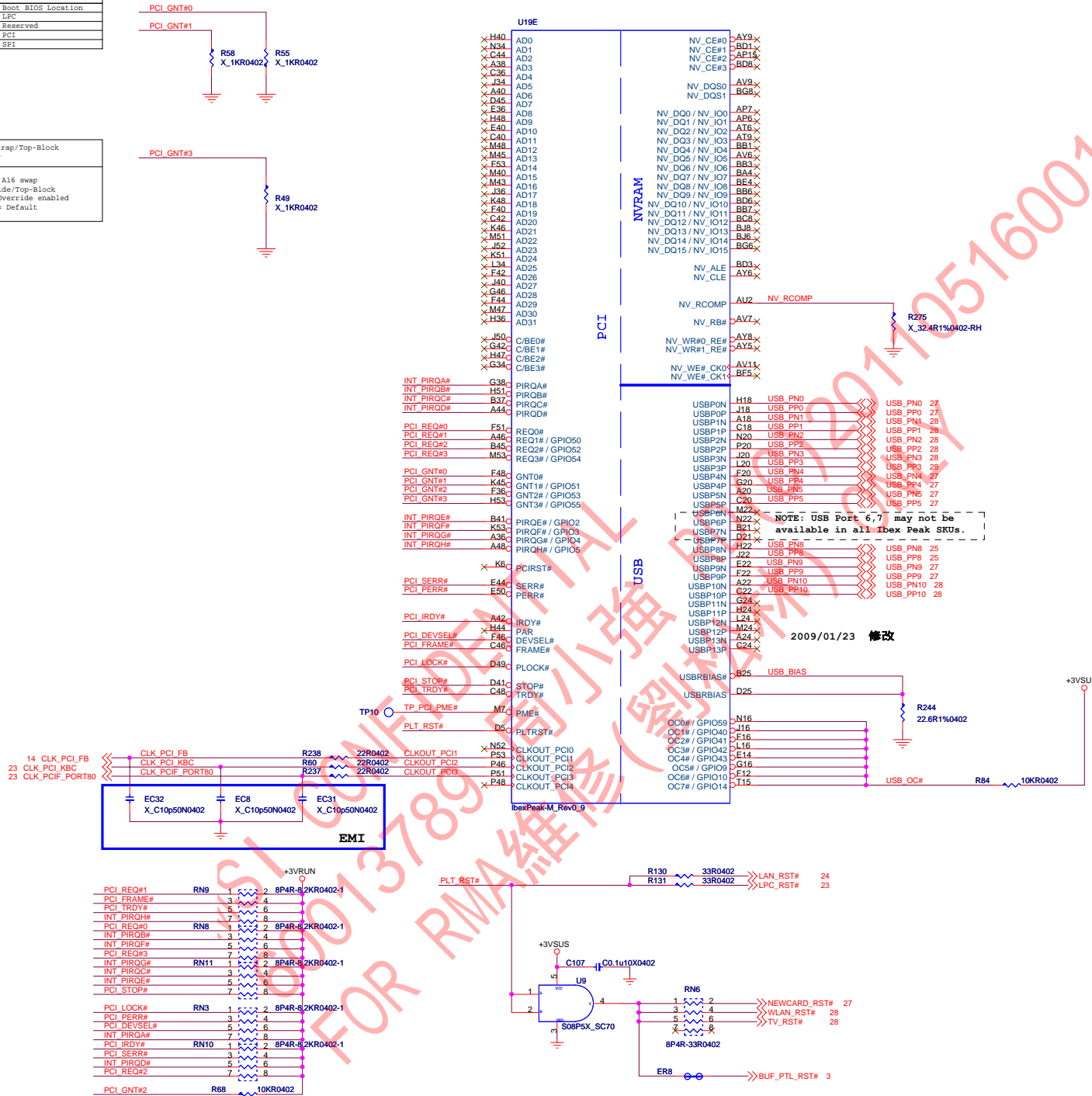




**IBEXPEAK - M (PCI,USB,NVRAM)**

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



The diagram illustrates the electrical connections for a device, organized into functional blocks. A large red watermark is present across the center, reading "600789 周小強 (周松林) 维修" and "FOR RMA 维修".

**Component List and Connections:**

Component	Function / Description	Connections
GPIO0	GPIO	Y0
C38	TACH1 / GPIO1	
D37	TACH2 / GPIO6	
J32	TACH3 / GPIO7	
HOST_ALERT#2	F10	GPIO8
PM_LANPHY_EN	K9	LAN_PHY_PWR_CTRL / GPIO12
HOST_ALERT#1	T7	GPIO15
AA2	SATA4GP / GPIO16	
F38	TACH0 / GPIO17	
02 BIOS_REC	Y7	SCLOCK / GPIO22
TP_UPEK_PWR_EN	H10	MEM_LED / GPIO24
SATA_PWR_EN#0	AB12	GPIO27
SPI_CS#2	V13	GPIO28
STP_PCI#	M11	STP_PCI# / GPIO34
SATA_PWR_EN#1	V6	SATACLKREQ# / GPIO35
AB7	SATA2GP / GPIO36	
AB13	SATA3GP / GPIO37	
MFG_MODE	V3	SLOAD / GPIO38
CRB_SV_DET	P3	SDATAOUT0 / GPIO39
SPI2_SO	H3	PCIECLKRQ6# / GPIO45
F1	PCIECLKRQ7# / GPIO46	
SV_SET_UP	AB6	SDATAOUT1 / GPIO48
CRIT_TEMP_REP#_R	AA4	SATA5GP / GPIO49
GPIO57	F8	GPIO57
A4	VSS_NCTF_1	
A49	VSS_NCTF_2	
A5	VSS_NCTF_3	
A50	VSS_NCTF_4	
A52	VSS_NCTF_5	
A53	VSS_NCTF_6	
B2	VSS_NCTF_7	
B4	VSS_NCTF_8	
B52	VSS_NCTF_9	
B53	VSS_NCTF_10	
BE1	VSS_NCTF_11	
BE53	VSS_NCTF_12	
BE1	VSS_NCTF_13	
BE53	VSS_NCTF_14	
BH1	VSS_NCTF_15	
BH2	VSS_NCTF_16	
BH52	VSS_NCTF_17	
BH53	VSS_NCTF_18	
B1	VSS_NCTF_19	
B12	VSS_NCTF_20	
B14	VSS_NCTF_21	
B149	VSS_NCTF_22	
B15	VSS_NCTF_23	
B150	VSS_NCTF_24	
B152	VSS_NCTF_25	
B153	VSS_NCTF_26	
D1	VSS_NCTF_27	
D2	VSS_NCTF_28	
D53	VSS_NCTF_29	
E1	VSS_NCTF_30	
E53	VSS_NCTF_31	

**Functional Blocks:**

- MISC:** Includes components like BMBUSY#, CLKOUT\_PCIE6N, CLKOUT\_PCIE6P, CLKOUT\_PCIE7N, CLKOUT\_PCIE7P, A20GATE, U2, H\_A20GATE, BCLK\_CPU#, BCLK\_CPU, H\_PECI, H\_PECI, KBRST#, H\_CUPWRGD, PCH\_THRMTRIP#\_R, R264, 56R1%0402.
- CPU:** Includes components like CLKOUT\_BCLK0\_N / CLKOUT\_PCIE8N, CLKOUT\_BCLK0\_P / CLKOUT\_PCIE8P, PECl, RCIN#, PROCPWRGD, THRMTRIP#, TP1, AW22, BB22, AY45, AY46, AV43, AV45, AF13, M18, N18, AJ24, AK41, AK42, M32, N32, M30, N30, H12, AA23, AB45, AB38, AB42, AB41, T39, INIT3\_3V#, TP24.
- NCTF:** Includes components like VSS\_NCTF\_1 through VSS\_NCTF\_31.
- RSVD:** Includes components like VSS\_NCTF\_1 through VSS\_NCTF\_31.

**Other Components:**

- Host Alerts:** HOST\_ALERT#1, HOST\_ALERT#2, R115, R102, R118, R95, R94, R92, X 1KR0402.
- Temperature and Power:** CRIT\_TEMP\_REP#\_R, R129, R132, 10KR0402, STP\_PCI#, 8P4R-10KR0402.
- SV Set Up:** SV\_SET\_UP, S\_GPIO0, MFG\_MODE, RN14, 1, 2, 3, 4, 5, 6, 8.
- CRB SV Det:** CRB\_SV\_DET, R286, R274, 10KR0402.

**Power and Grounding:**

- +VTT:** Connected to VSS\_NCTF\_1 through VSS\_NCTF\_31.
- +3VSUS:** Connected to VSS\_NCTF\_1 through VSS\_NCTF\_31.
- +3VRUN:** Connected to VSS\_NCTF\_1 through VSS\_NCTF\_31.

**Legend:**

- Host Alerts:** HOST\_ALERT#1, HOST\_ALERT#2, R115, R102, R118, R95, R94, R92, X 1KR0402.
- Temperature and Power:** CRIT\_TEMP\_REP#\_R, R129, R132, 10KR0402, STP\_PCI#, 8P4R-10KR0402.
- SV Set Up:** SV\_SET\_UP, S\_GPIO0, MFG\_MODE, RN14, 1, 2, 3, 4, 5, 6, 8.
- CRB SV Det:** CRB\_SV\_DET, R286, R274, 10KR0402.

**ibexPeak-M\_Rev\_9**

```
| Retain 25-MHz crystal footprint on your platform.
```

```
| ---Though FCIM will not be available, retaining the footprint will allow
```

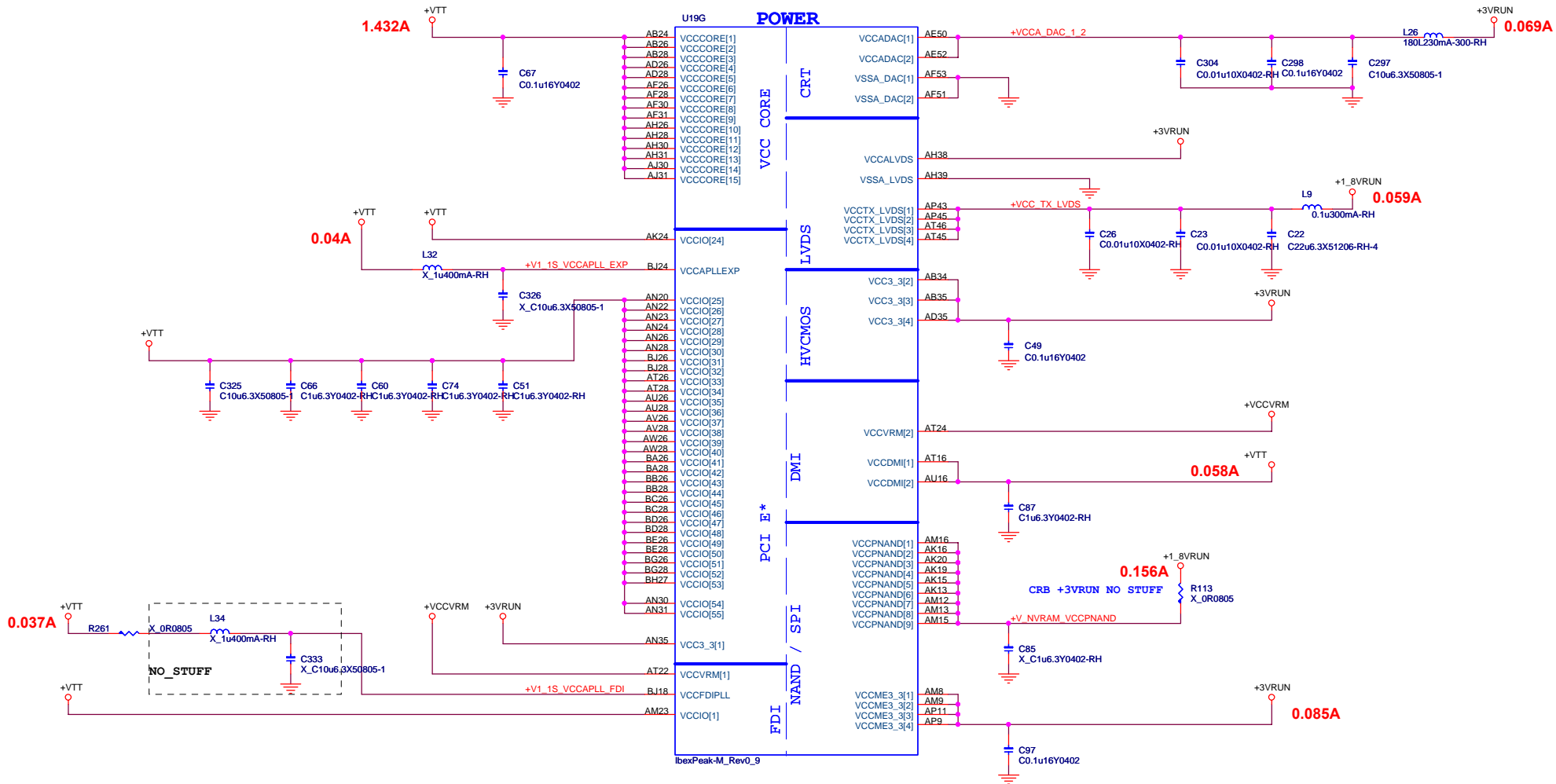
```
| Intel and customer to test and evaluate FCIM for future platforms.
```

```
| ---25-MHz crystal and associated capacitor footprints only are requested
```

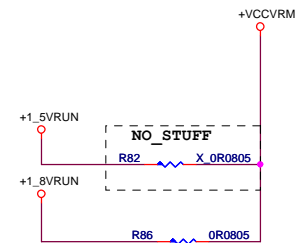
```
N | components do not need to be populated.
```

```
| ---Keep 1K Ohm resistor un-stuffed to GND on Ibex Peak GPIO8.
```

# IBEXPEAK - M (POWER)

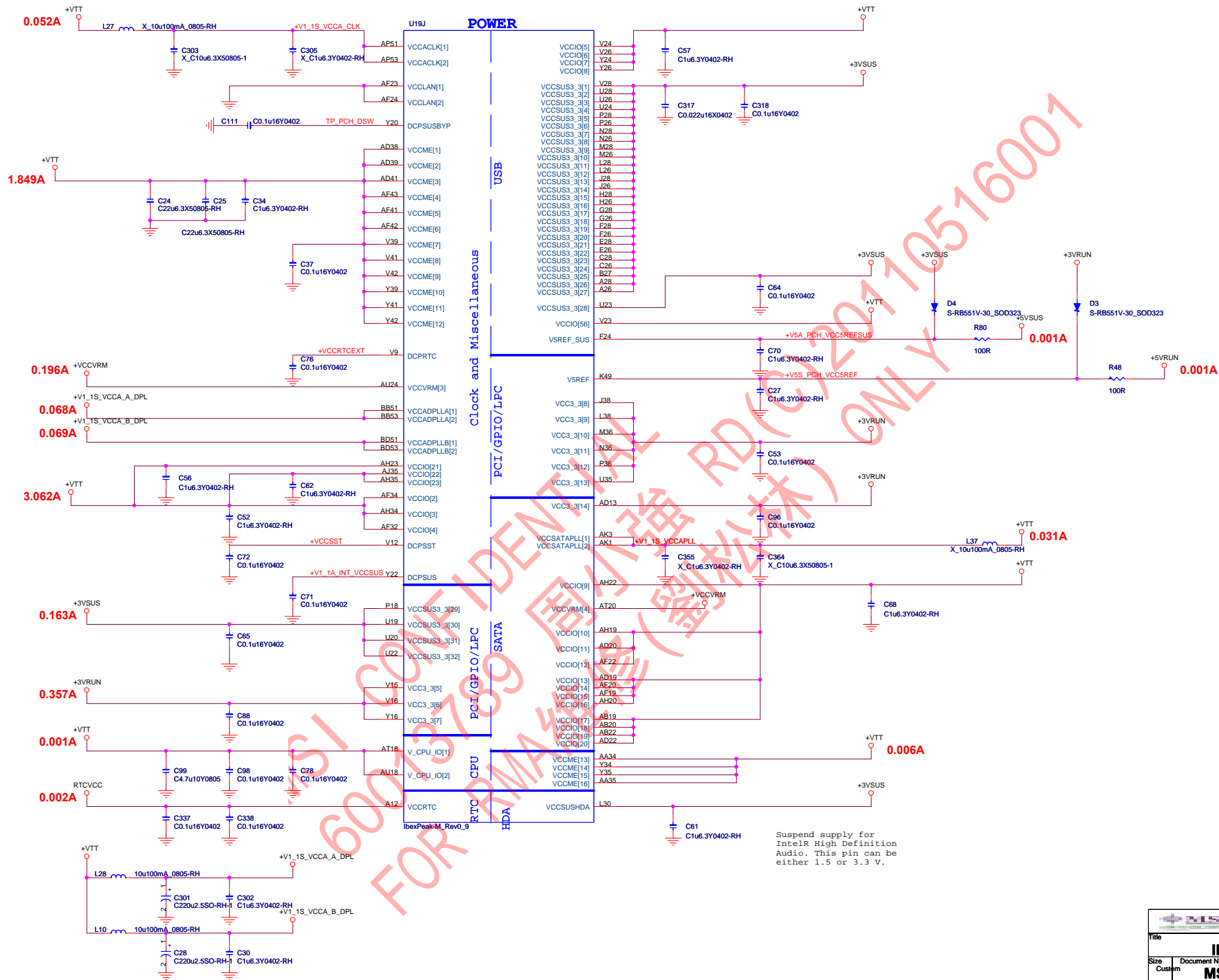


The VCCVCRM rail (1.8 V/1.5 V) powers an internal voltage regulator module (VRM) that regulates clean 1.05-V voltage supply for analog rails (VCCAClk, VccapllEXP, VCCFDIPLL, and VCCSATAPLL). This solution will allow us to remove the LC filter requirements for those rails, thereby reducing platform BOM cost. VCCVCRM is enabled by default via internal pull up to GPIO27, therefore GPIO27 should be left as No Connect. The following diagram shows implementation details on how to enable and disable VccVRM.

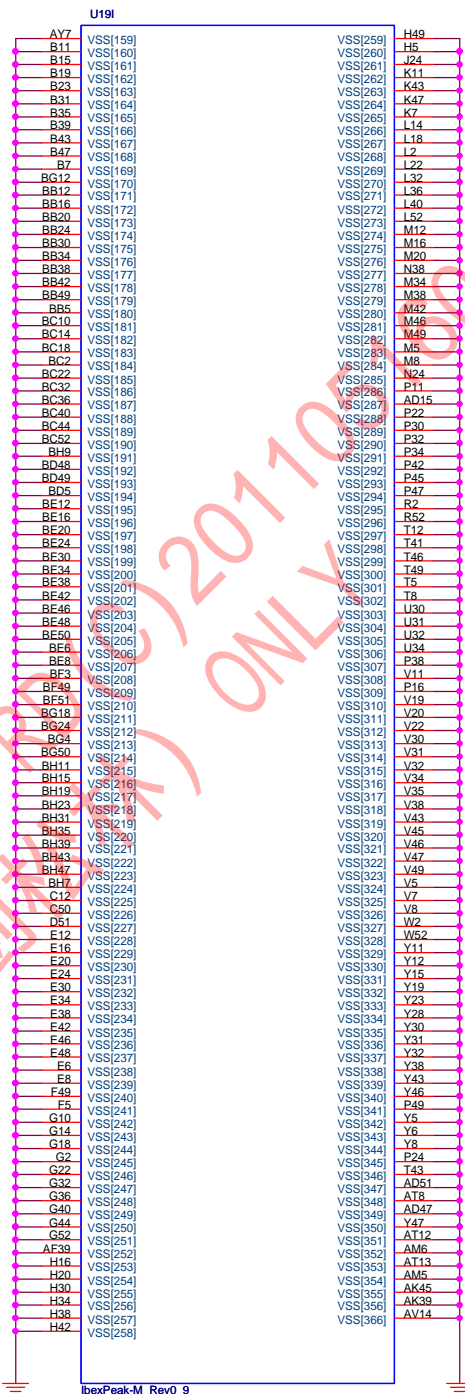
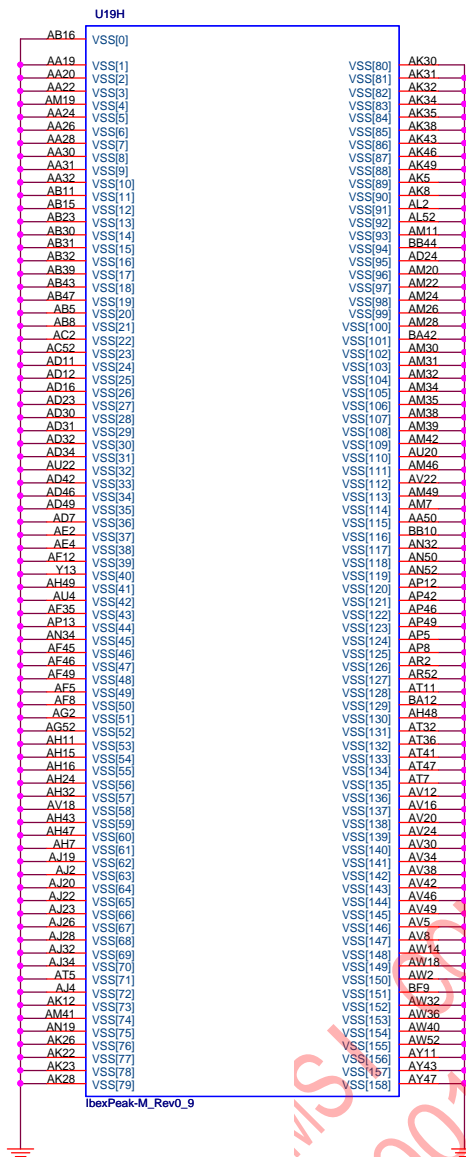


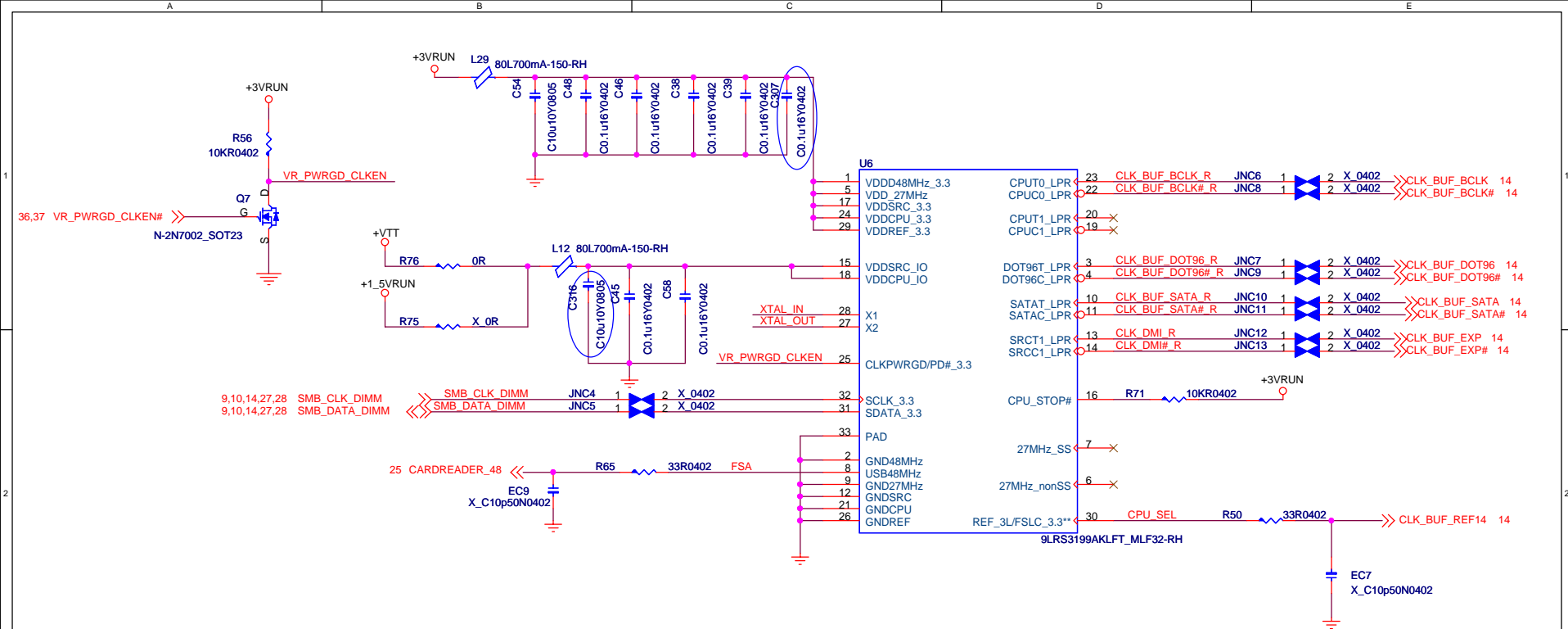
VccLAN may be grounded if Intel LAN is disabled.

# IBEXPEAK - M (POWER)



# IBEXPEAK - M (GND)

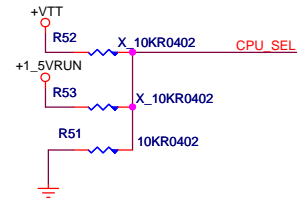
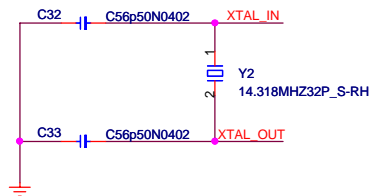




For CPU frequency select (133MHz)

### Capacity select

If LC=20pf C708/C709=33pf  
If LC=32pf C708/C709=56pf

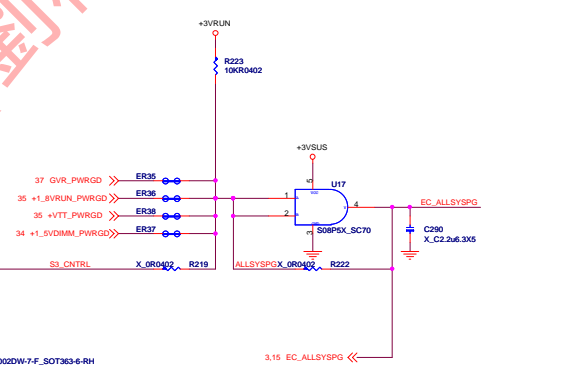
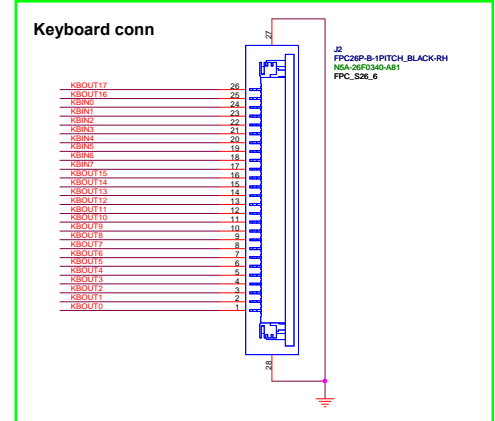
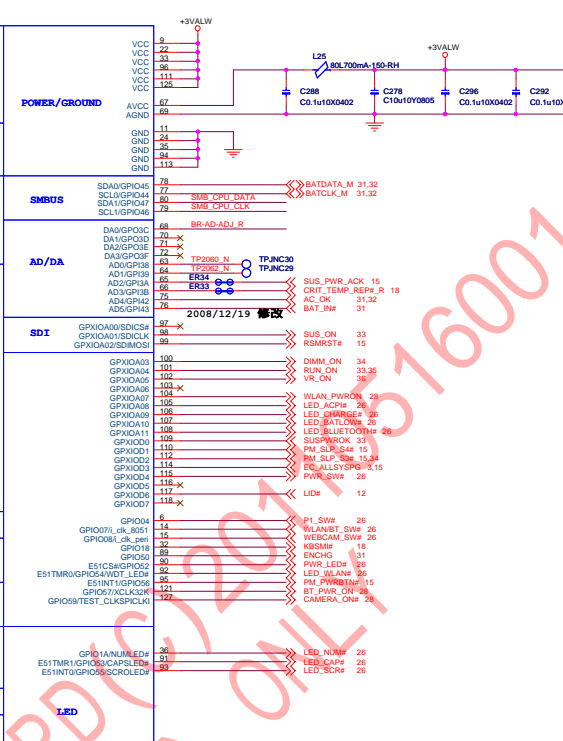
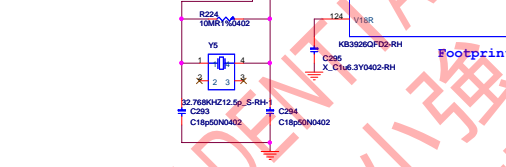
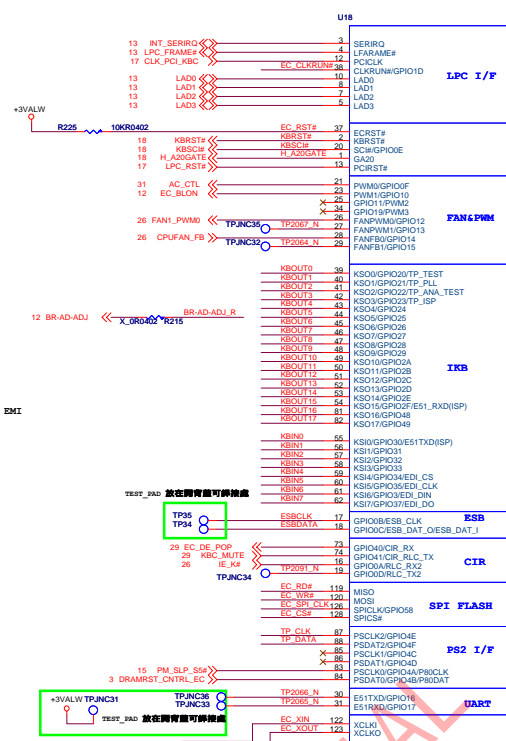
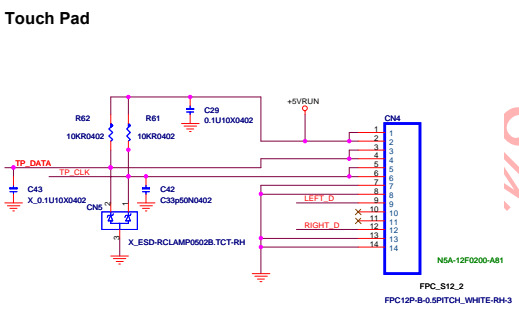
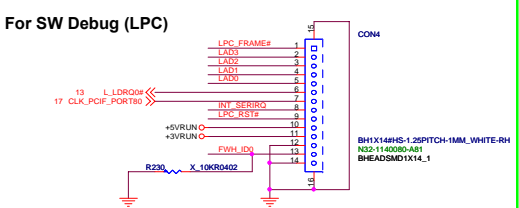
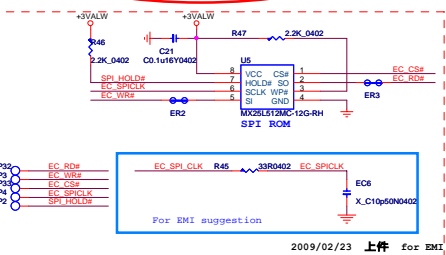


CPU_SEL	CPU0	CPU1
0(Default)	133MHz	133MHz
1(1.05~1.5V)	100MHz	100MHz

### Co-Lay Note:

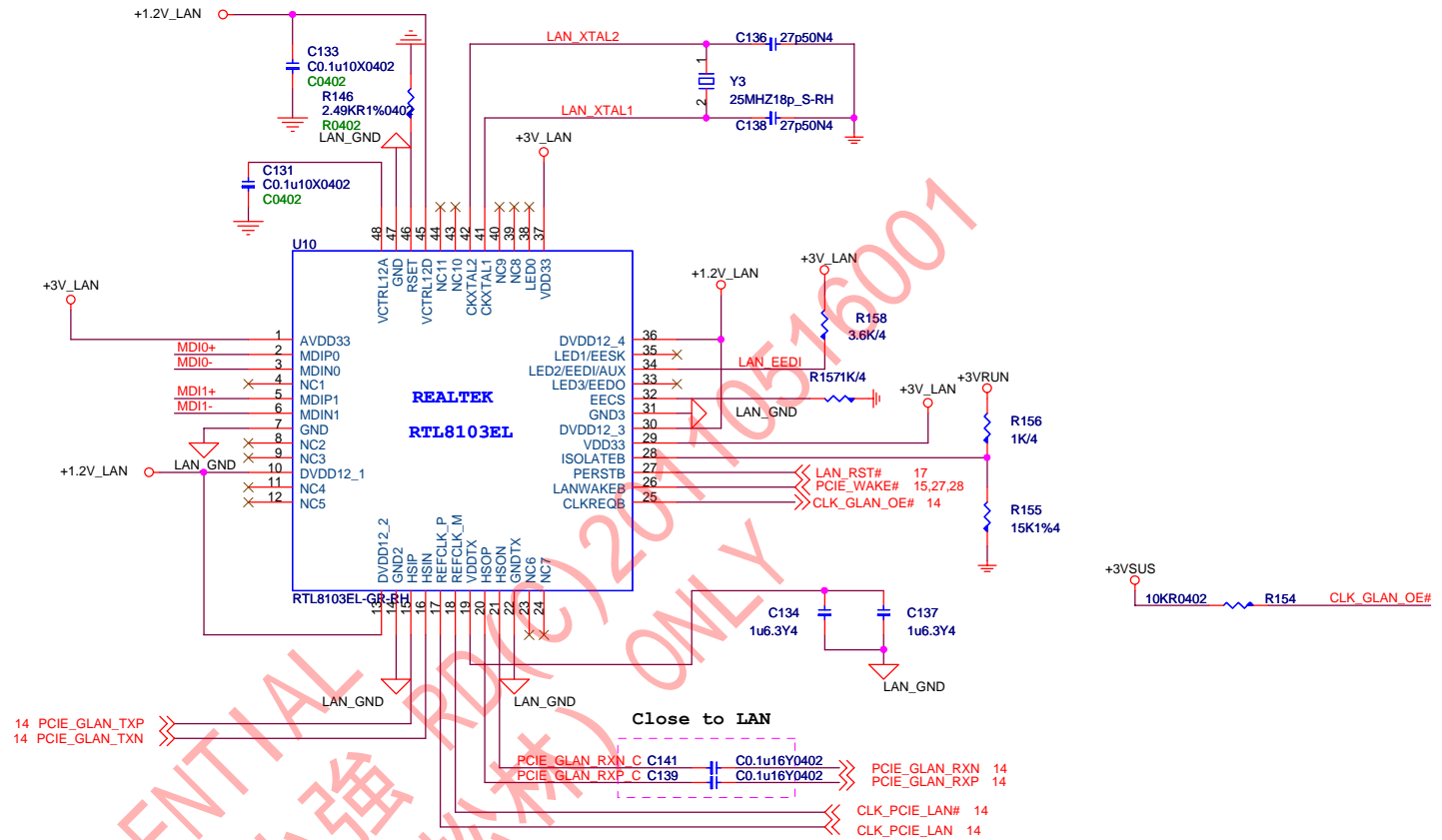
For IDT IC9IRS3199  
R598,R599,R600=10Kohm

For Sillego SLG8SP587  
R598,R599,R600=4.7Kohm



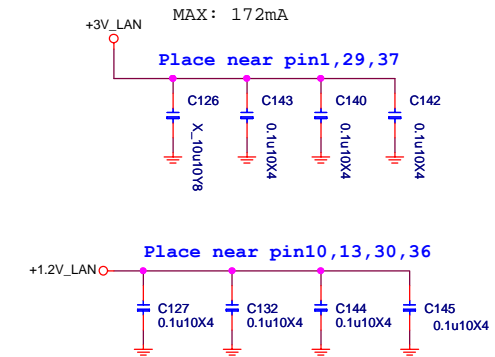
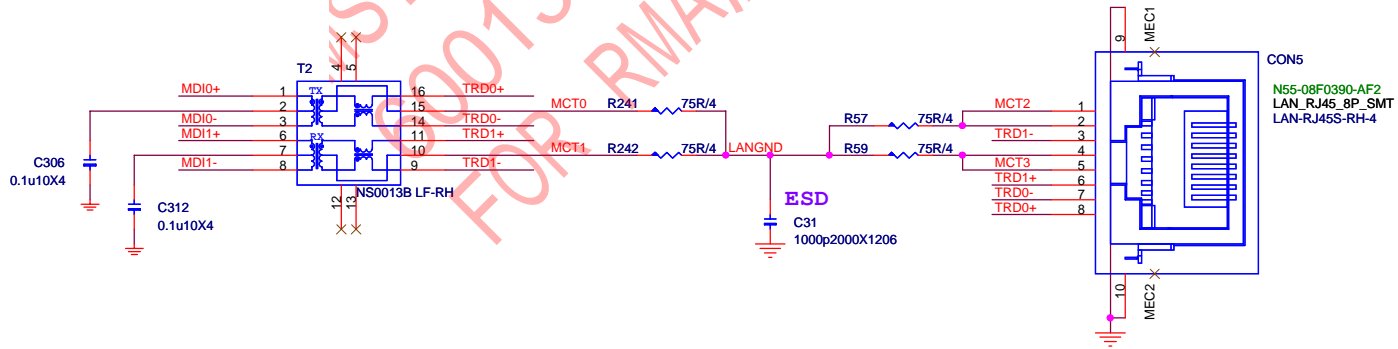


1. Pin 46 : RSET res. should be close to LAN chip. Don't have power trace or high frequency trace beside it.
2. The trace of each Pair(MDIX+/-) should be equal in length and better have ground under.
3. Both EGND and GND can be connect together or use 0 Ohm res. to connect them.
4. 1.2V請留 power plane並且盡量大一點.
5. 1.2V Bypass 電容不能省. 在 LAN 的每一個 power pin 都加 0.1u 的電容, 不能省.
6. 請參考RTL8111C EMI layout notice. Fine tune cap (0.1uF ~ 10pF) of center-tapped can improve EMI for single tone noise.
7. Please refer and follow our Layout Guidel.5 as attached file
8. RJ45 的部份,對應pin 請您在confirm一下.....一般都是接到 RJ45 pin 12/ 36

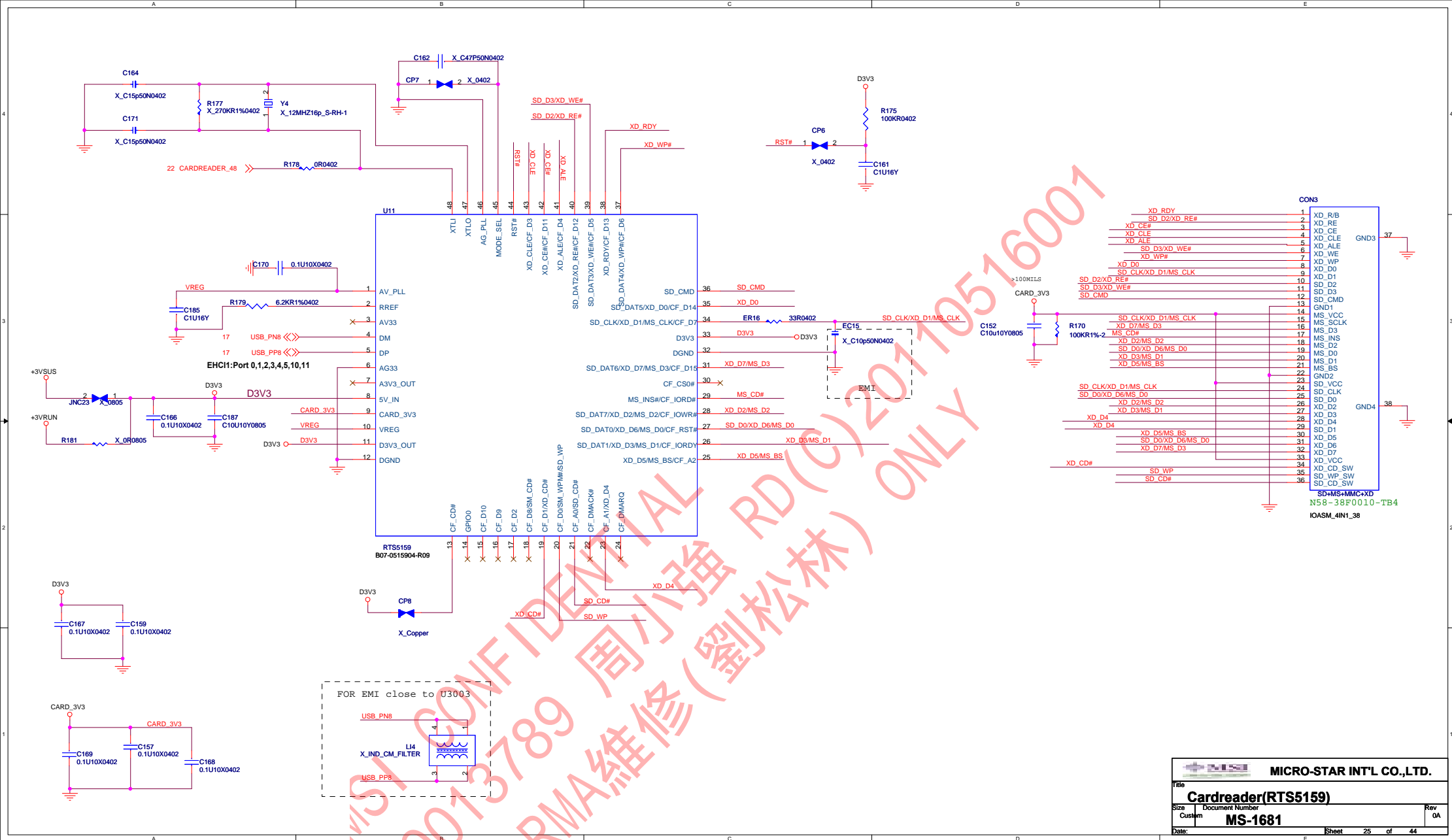


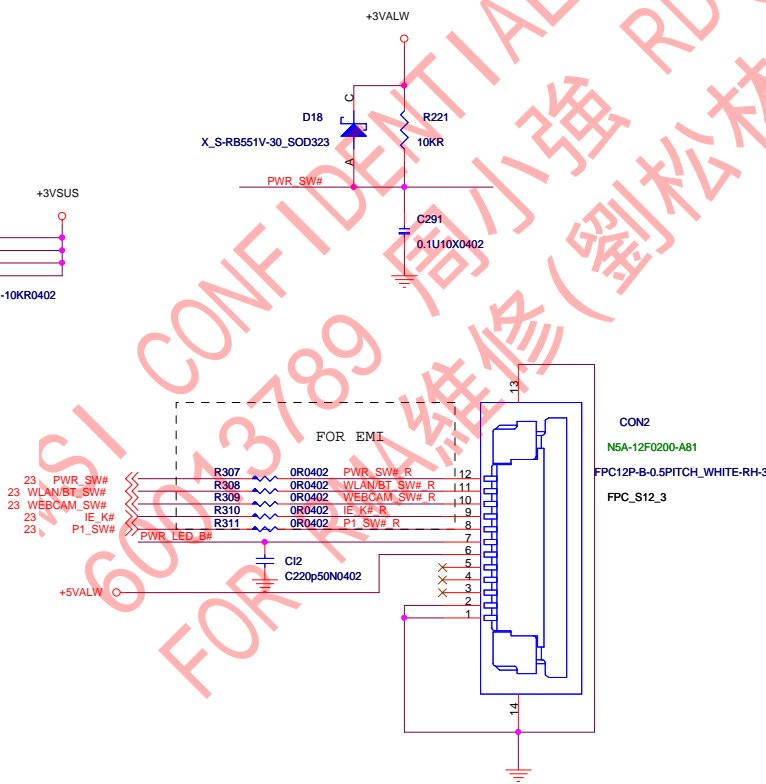
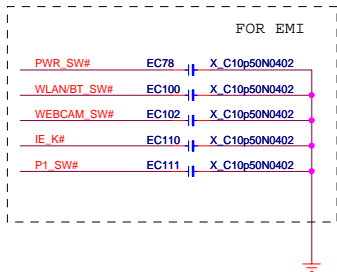
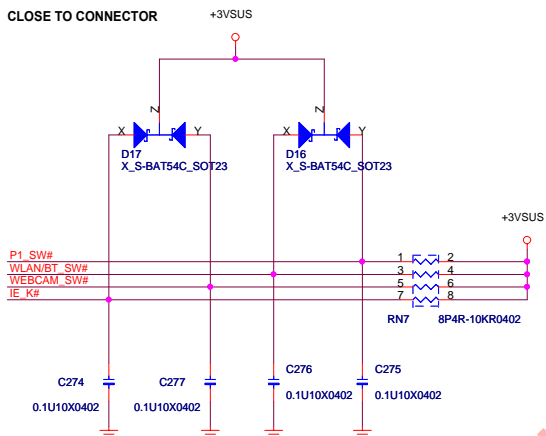
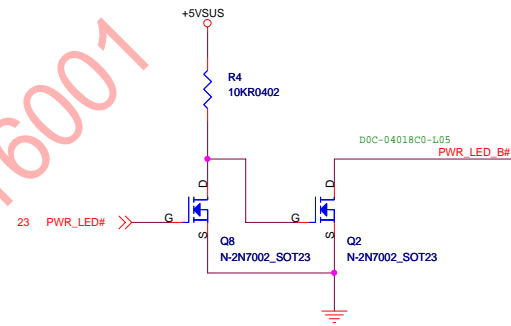
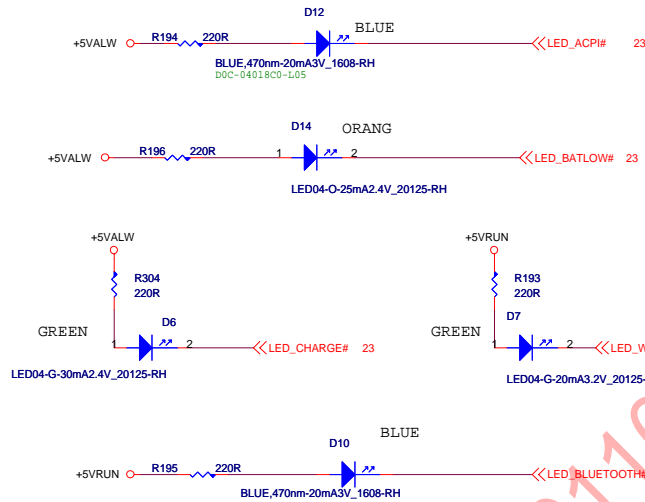
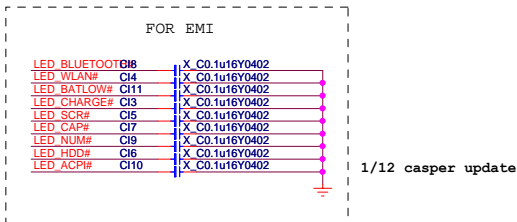
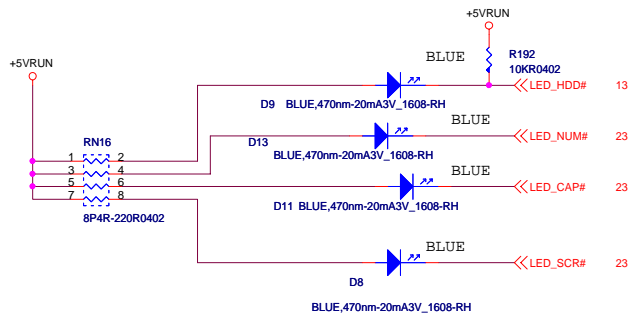
#### POWER Comparison

	3.3V	mW
10 M Idle/TxRx	87/172	287/568
100 M Idle/TxRx	112/165	370/545
ALDPS	60	198
D3 cold with link10M /without link	32/18	106/59.4

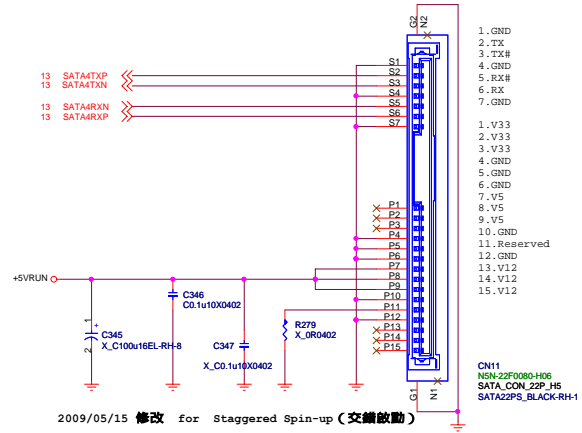




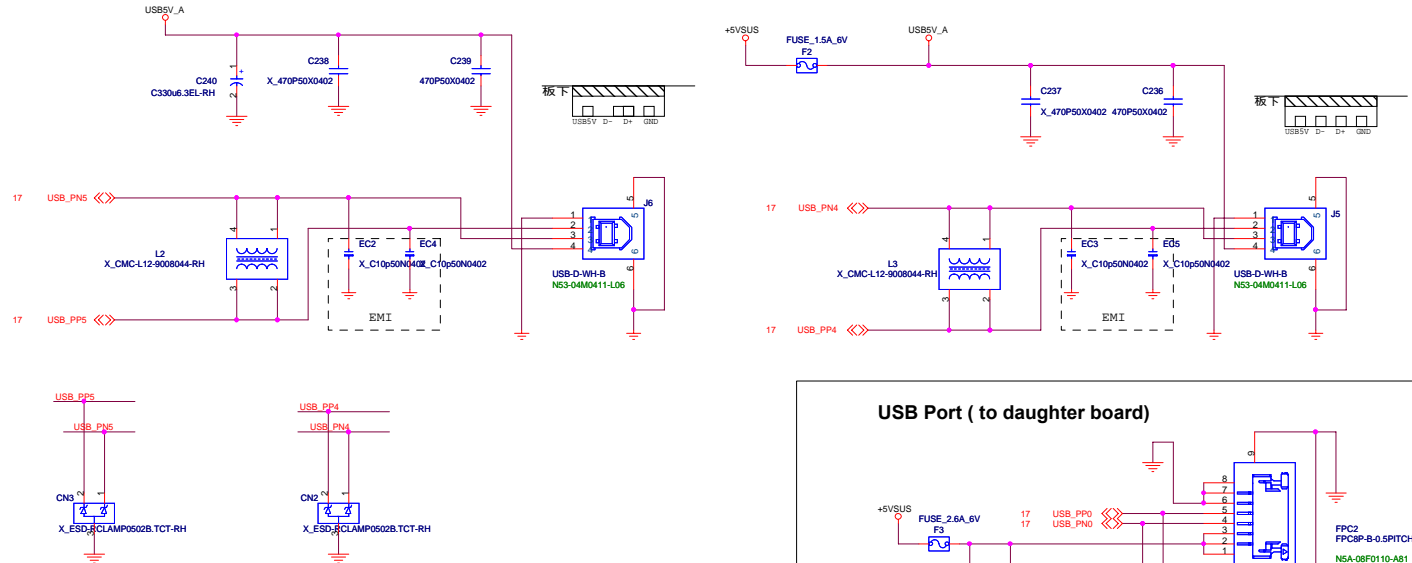




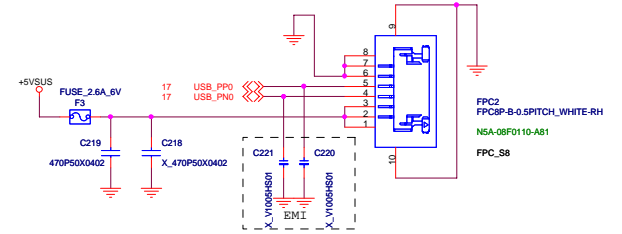
### SATA HDD



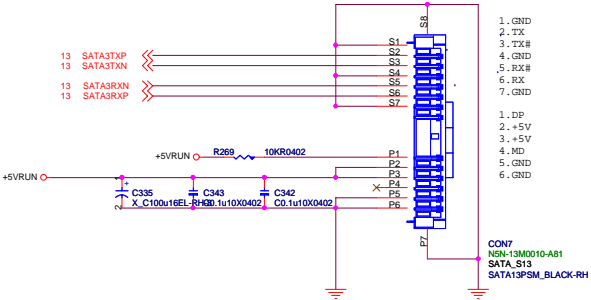
## USB Port



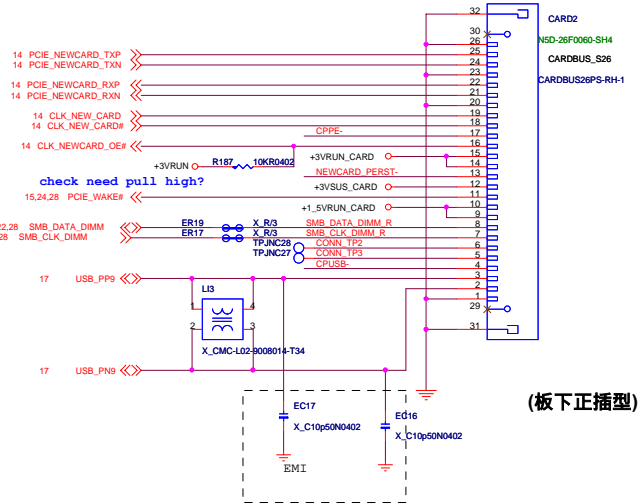
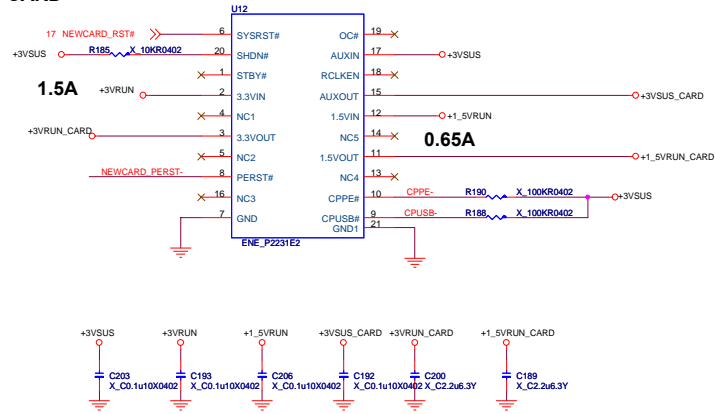
**USB Port ( to daughter board)**



## SATA ODD

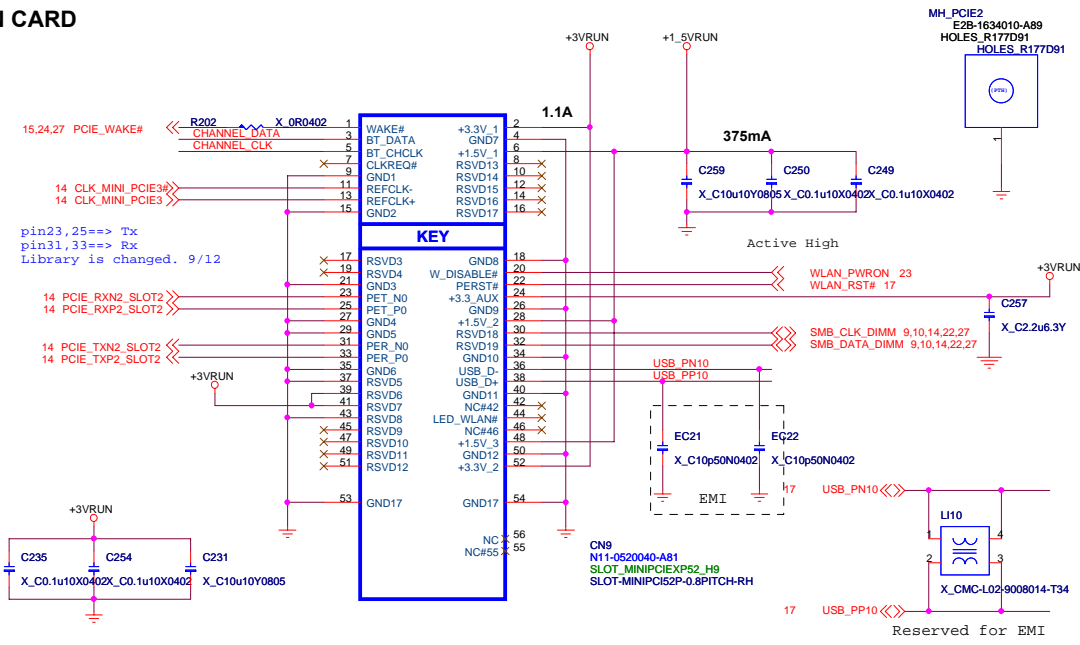


## NEW CARD

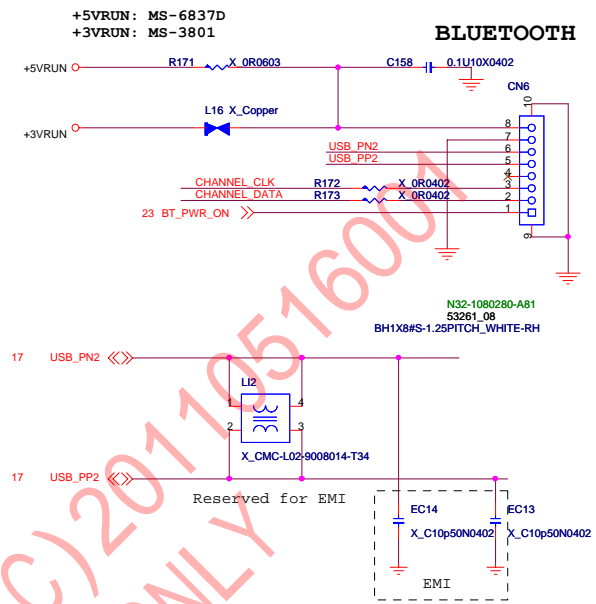


(板下正插型)

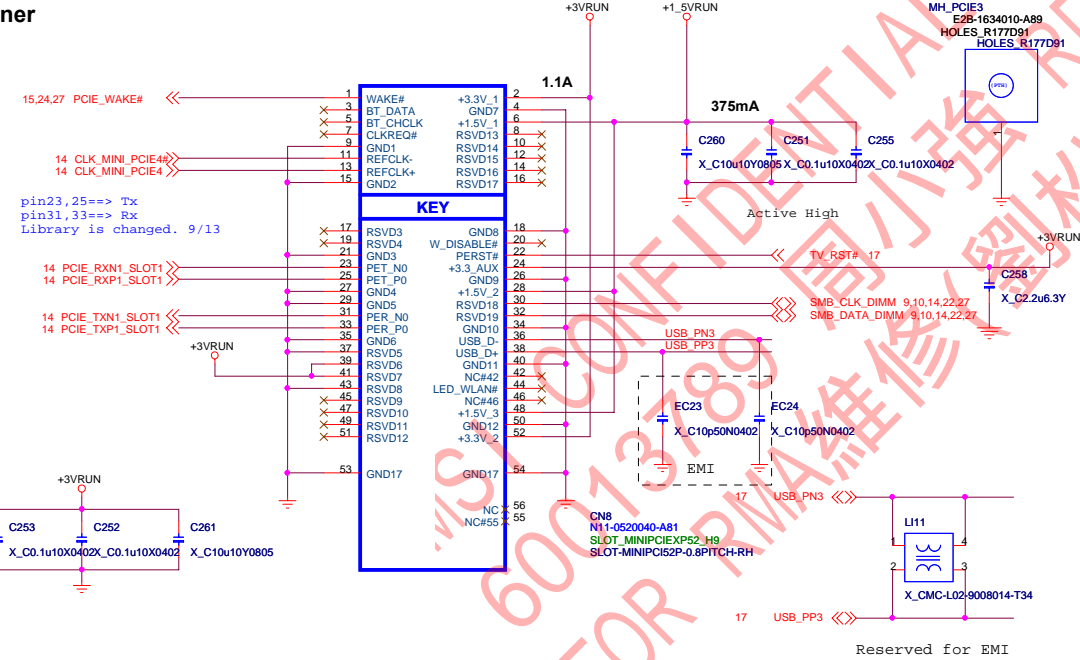
## WLAN CARD



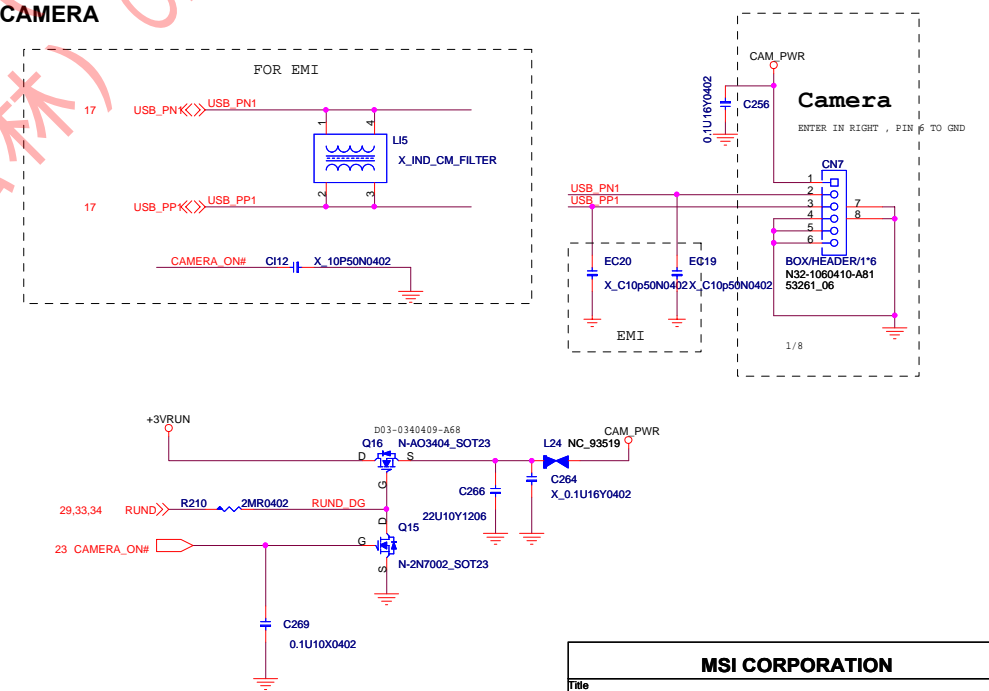
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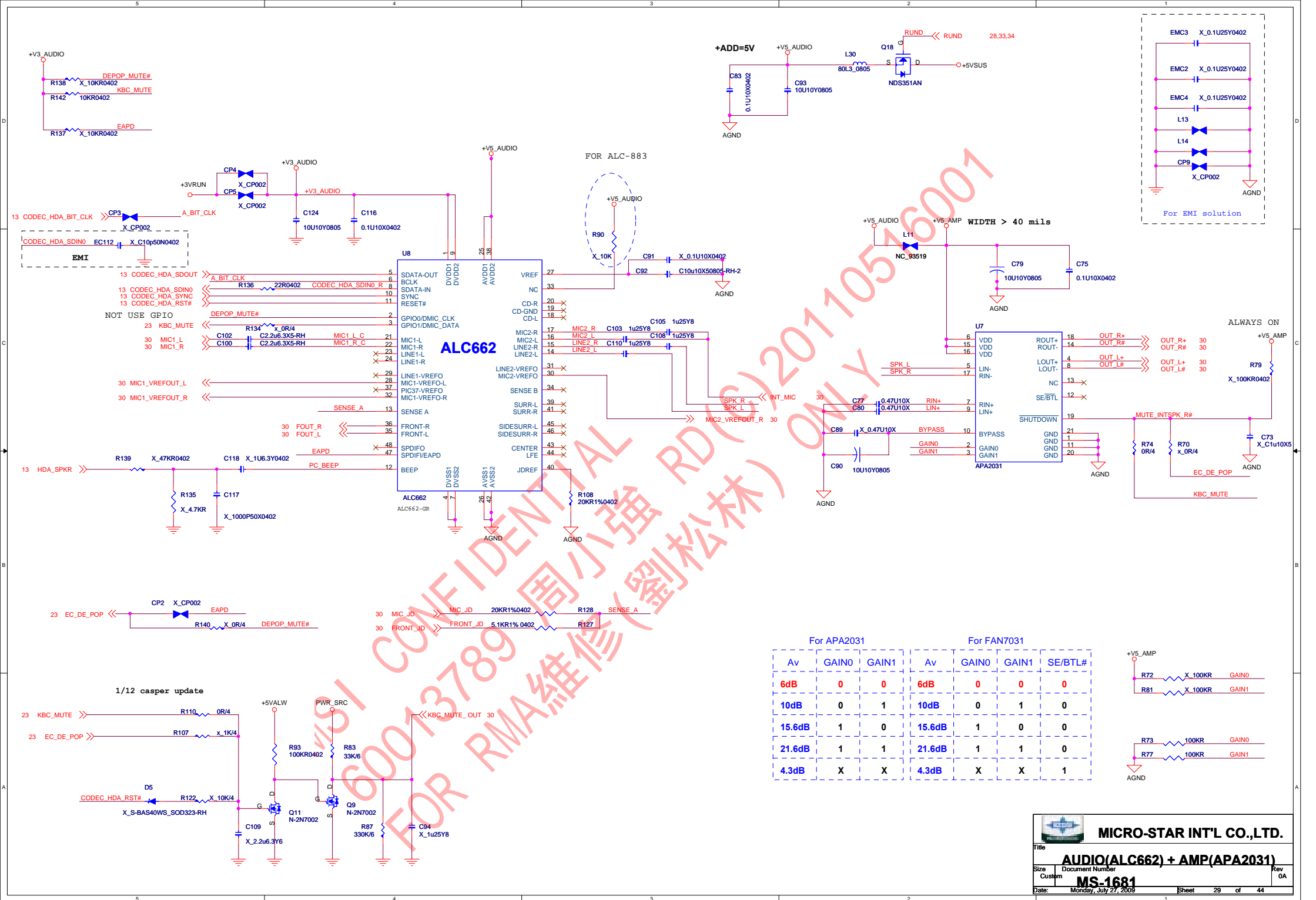


## TV Tuner

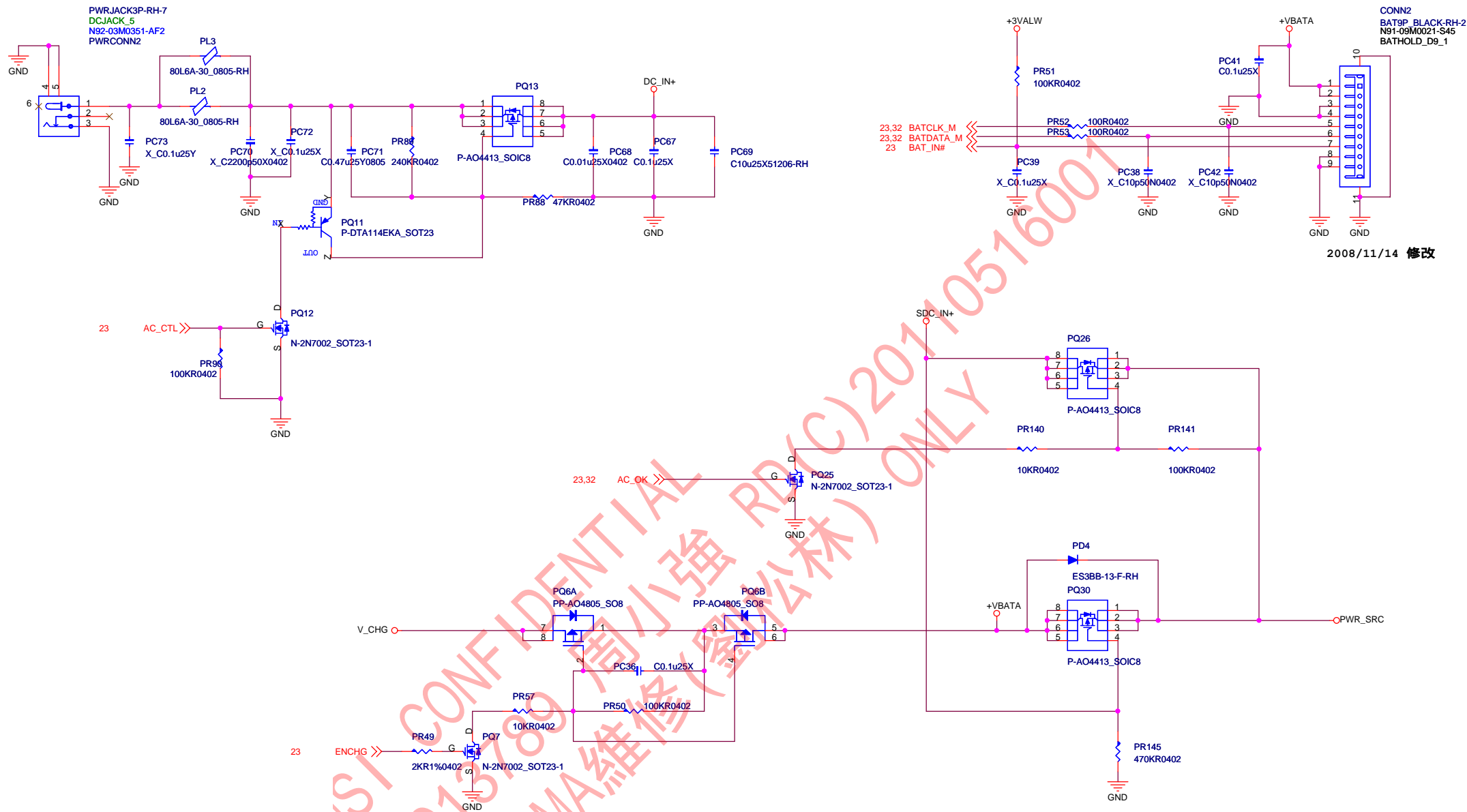


**CAMERA**






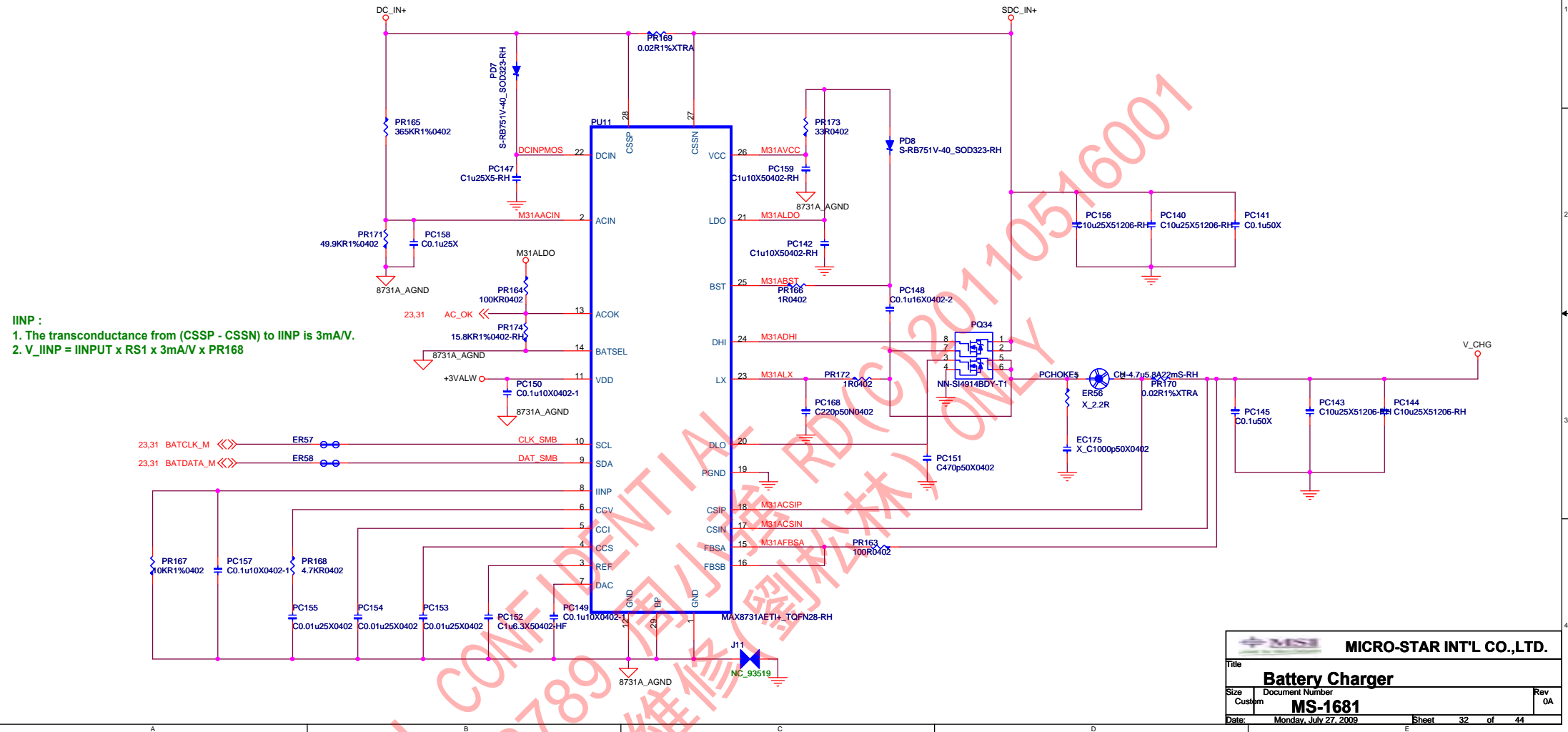




2008/11/14 修改

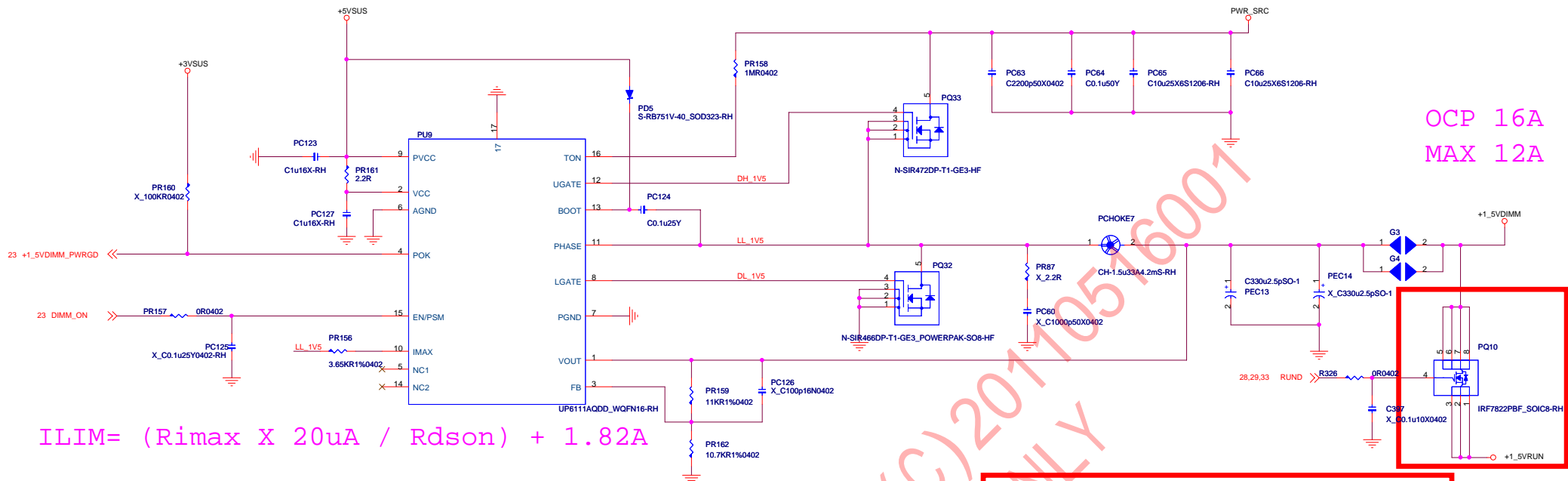
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Title					
Battery Select					
Size	Document Number		Rev		
Custom	MS-1681		0A		
Date:	Monday, July 27, 2009	Sheet	31 of 44		

Adapter= 65W  
Adapter input voltage set 19 Voltage

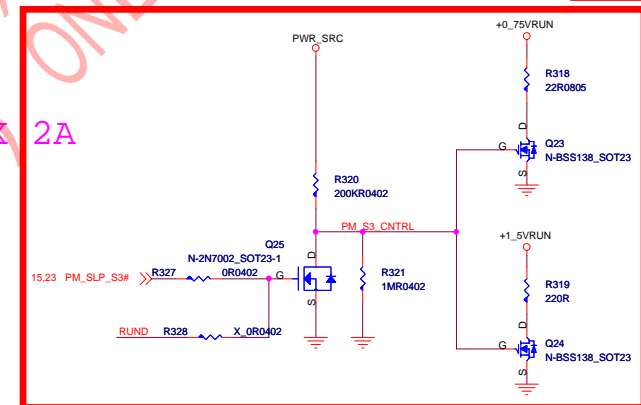




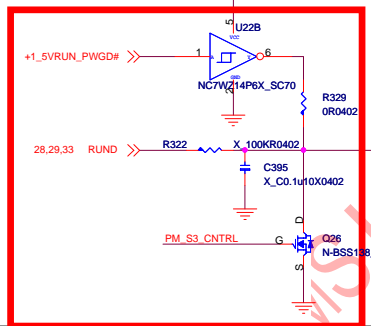




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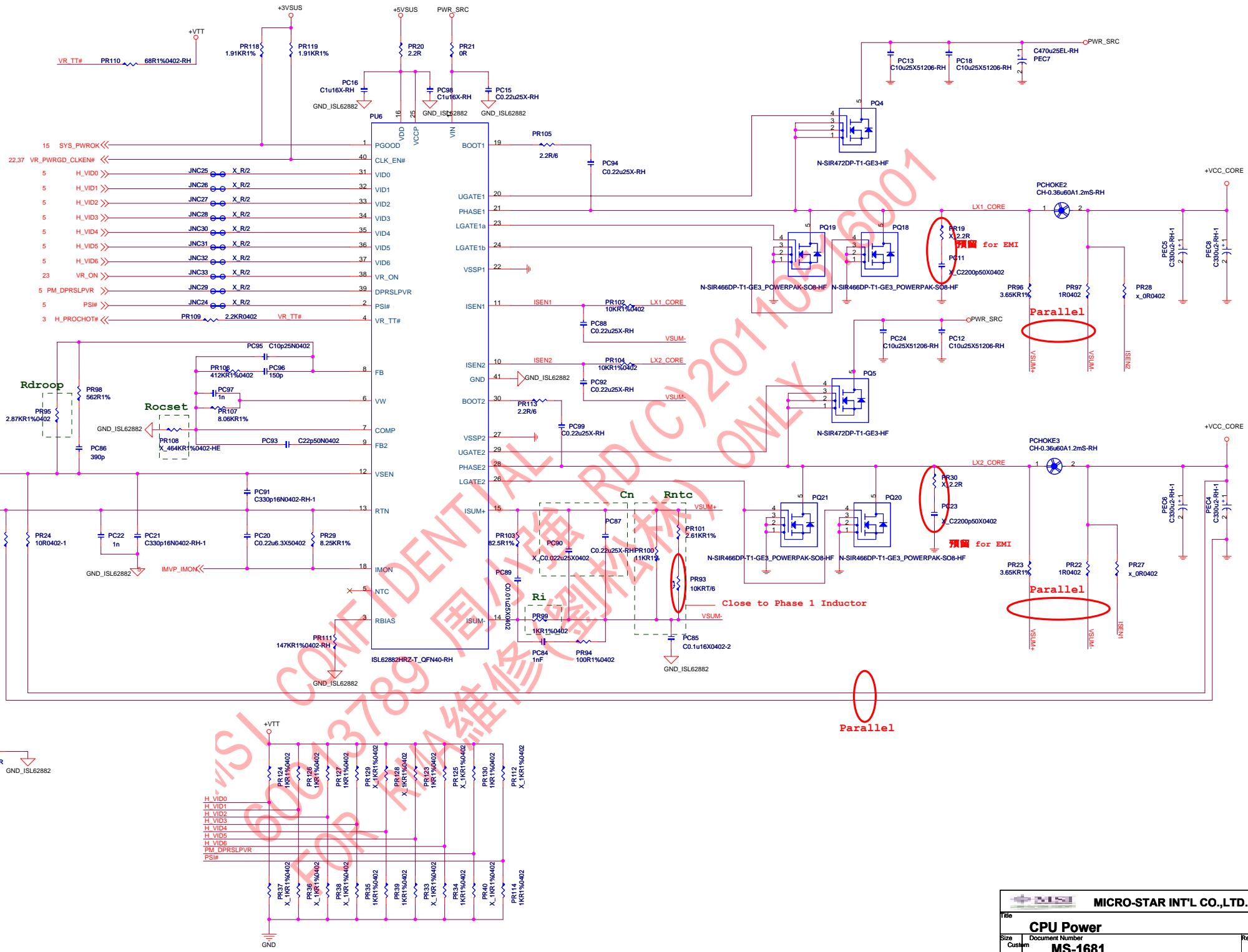
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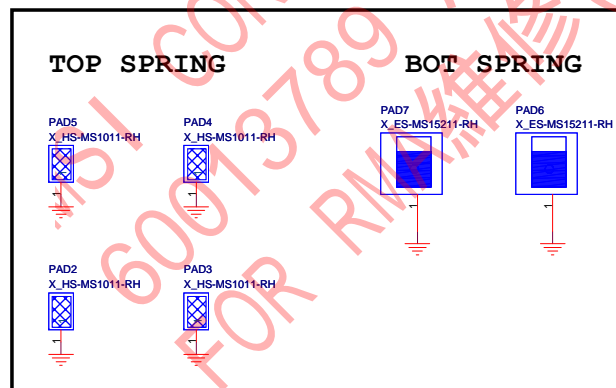
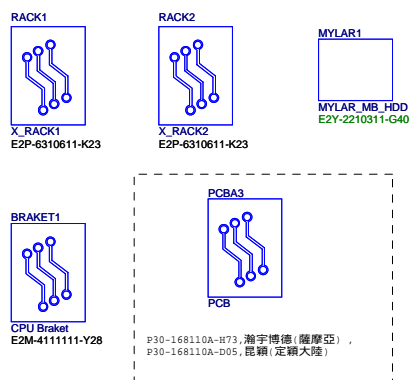
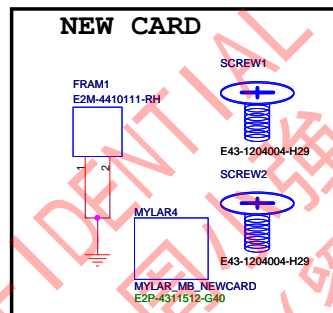
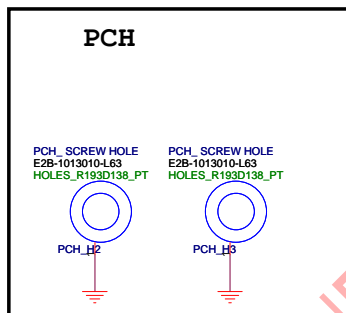
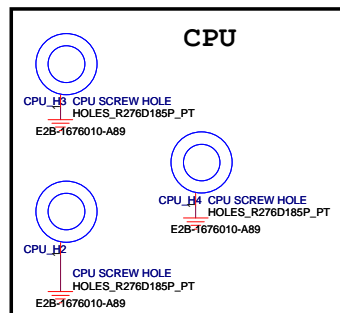
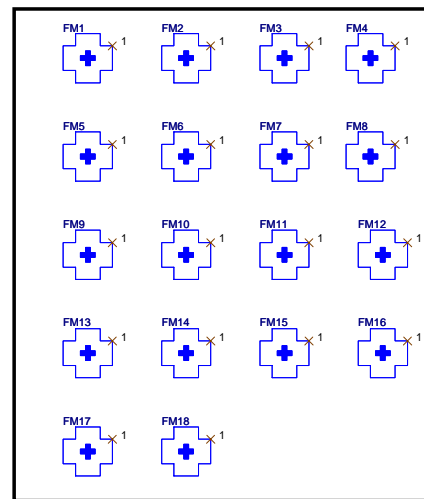
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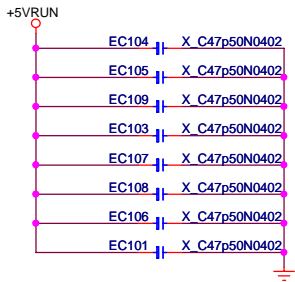
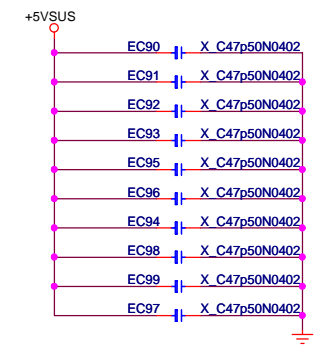
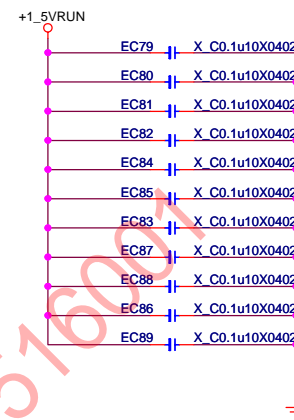
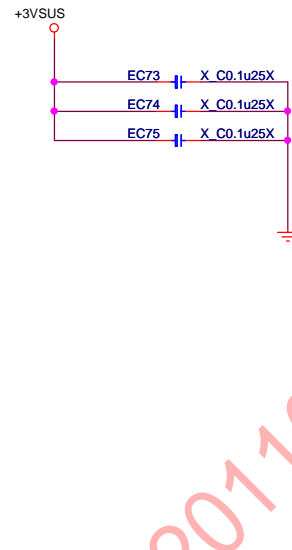
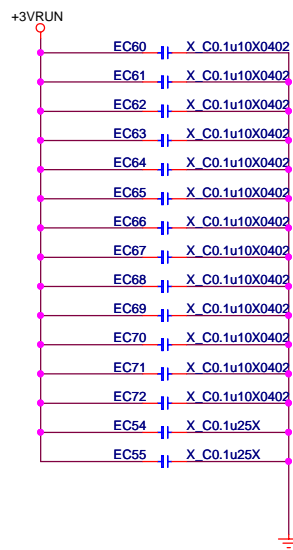
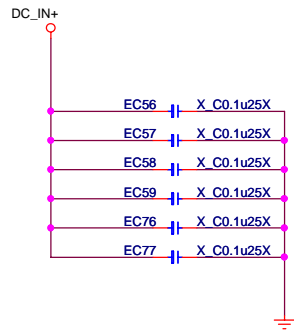
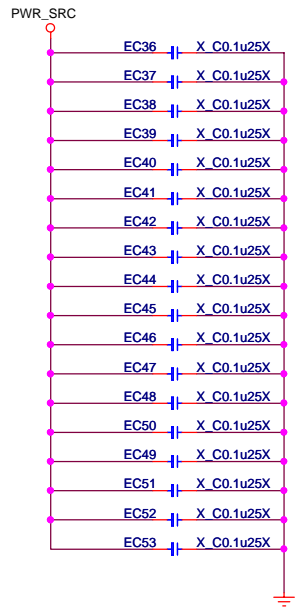
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Date:	Monday, July 27, 2009	Sheet	34 of 44







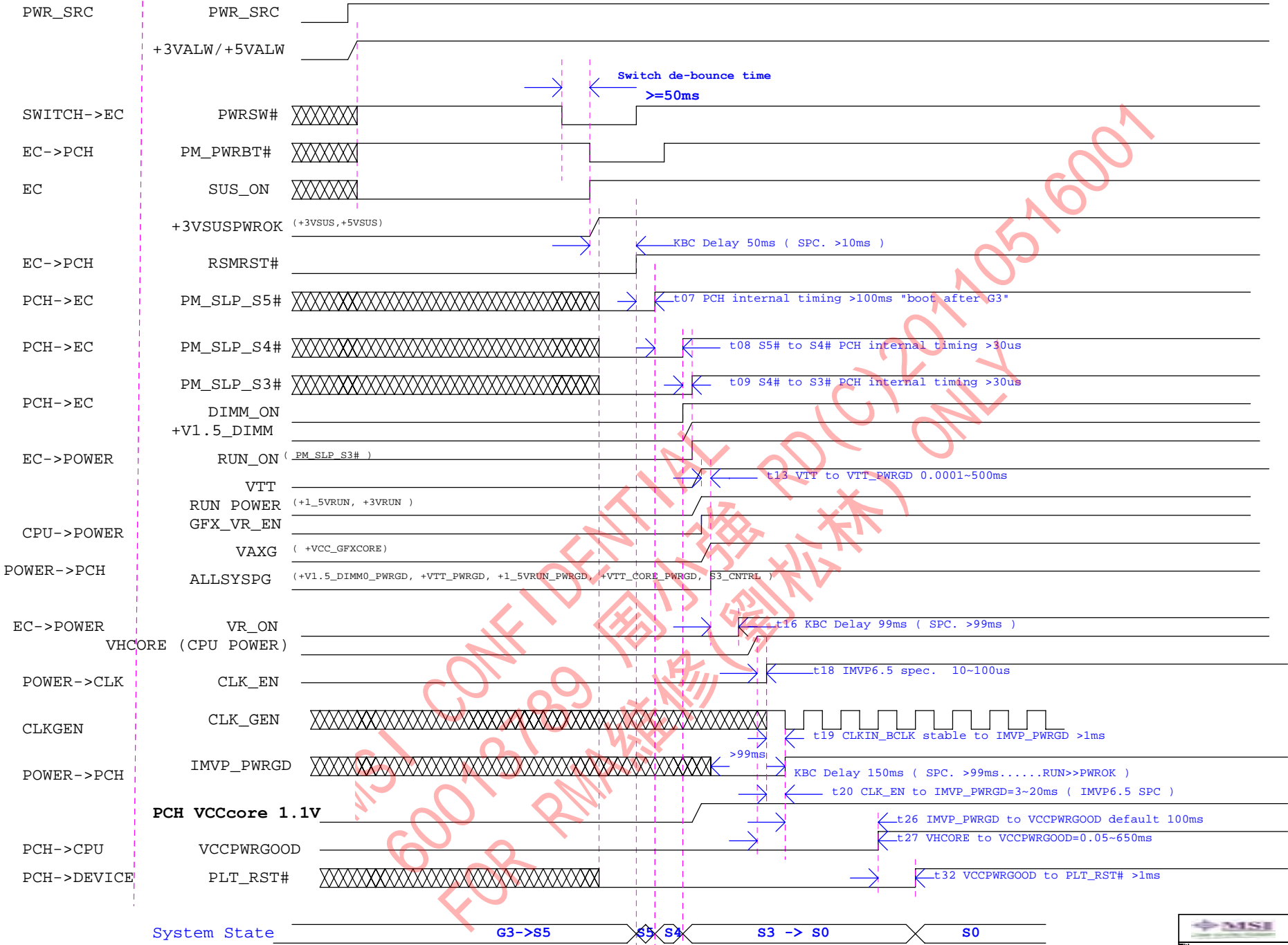




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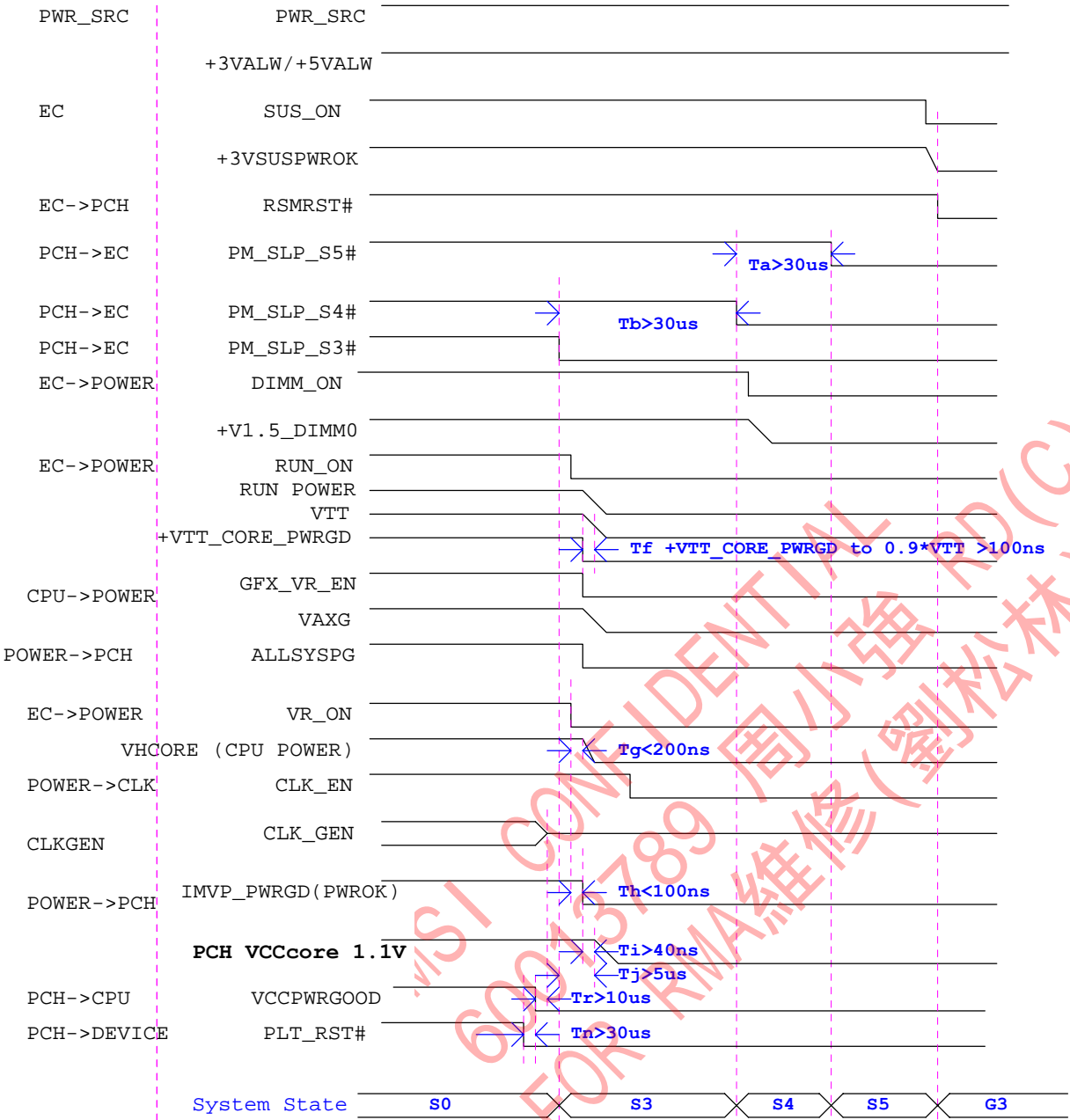
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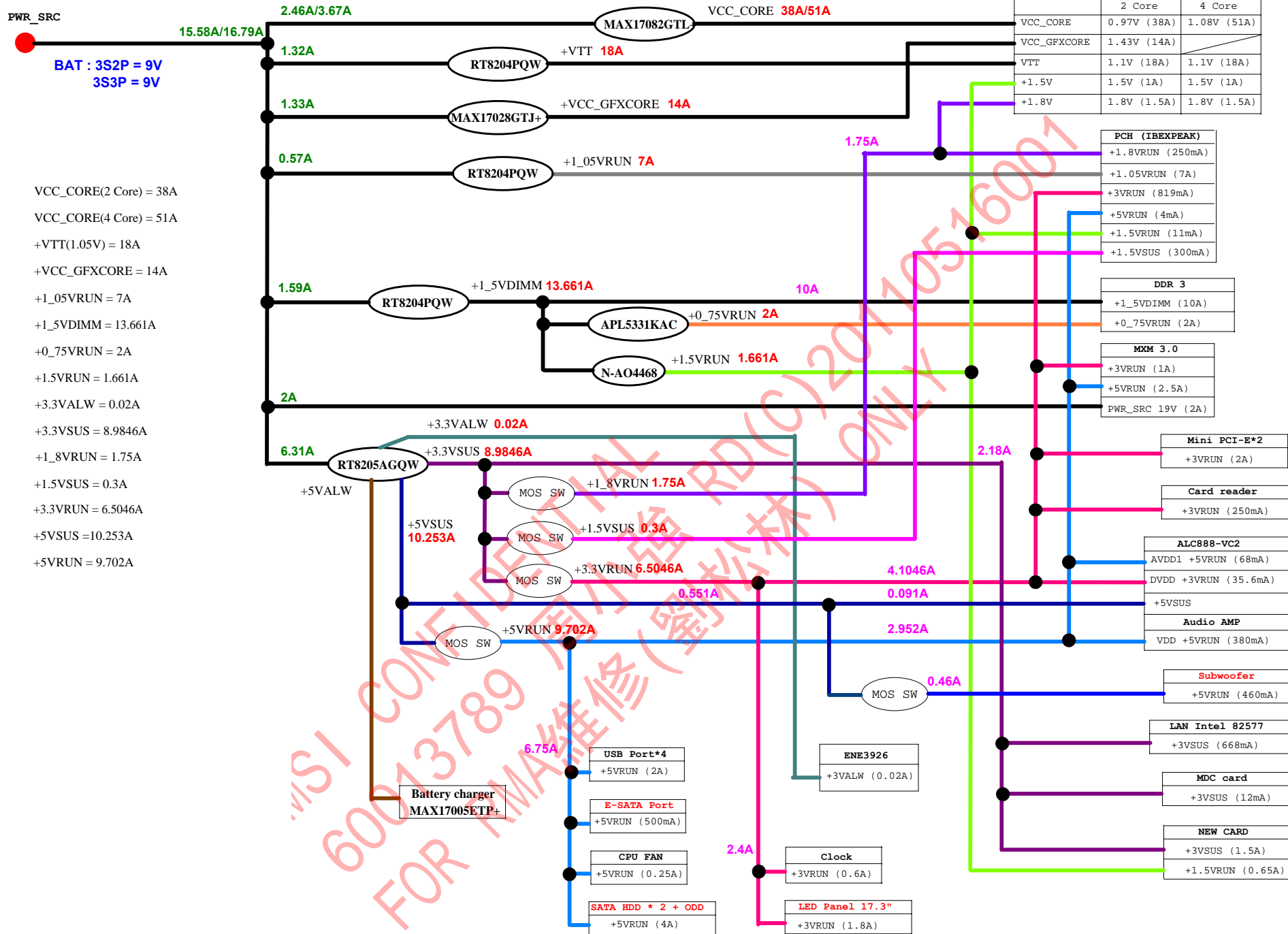
Calpella System Power on Sequence DC mode





Power down Sequence DC mode S0 to G3





2008/11/13 修改